Electronics and Electrical Engineering

AIMS Electronics and Electrical Engineering, 10(3): 446–472
DOI: 10.3934/electreng.2026018
Received: 27 November 2025
Revised: 13 March 2026
Accepted: 23 April 2026
Published: 09 June 2026

https://www.aimspress.com/journal/ElectrEng

Research article

Promotion of anti-disturbance capability in UPQC systems under FCS-MPC control with LADRC-optimized phase-locked loop

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Abstract: In three-phase three-wire power systems, unified power quality conditioners (UPQCs) compensate for current/voltage fluctuations while enhancing load-side power quality. However, current solutions face three key limitations: (1) limited responsiveness to rapid disturbances, (2) sensitivity to grid variations, and (3) inadequate phase-locked loop (PLL) performance, all of which undermine compensation effectiveness. Traditional proportional-integral (PI) controllers further exacerbate these issues through overshooting during control quantity disturbances. This paper proposes an enhanced finite control set model predictive control (FCS-MPC) system integrated with linear active disturbance rejection control (LADRC) to improve UPQC's anti-disturbance capabilities. The architecture combines a series active power filter (APF)-side voltage compensation module based on FCS-MPC, a shunt APF-side current compensation module based on FCS-MPC, and a LADRC-optimized mixed second/third-order generalized integrator-based PLL (MSTOGI-PLL). Through rigorous MATLAB/Simulink simulations, the proposed UPQC demonstrates superior robustness compared to conventional controllers, achieving 85% voltage sag compensation within 12.5 ms response time. Simulation result validation confirms that the LADRC-enhanced FCS-MPC system significantly improves disturbance rejection, yielding effectively reduced voltage total harmonic distortion (THD) and enhanced post-compensation power quality across various grid anomalies.

Keywords: unified power quality conditioner; finite control set model predictive control; linear active disturbance rejection control; mixed second- and third-order generalized integer; phase locked loop; anti-disturbance

1. Introduction

The incorporation of nonlinear loads and renewable energy equipment significantly impacts power quality on the load side of power systems. Variable frequency drives, rectifiers, and electronic equipment are nonlinear loads that draw current in non-sinusoidal patterns, resulting in harmonic distortion, voltage fluctuations, and electrical noise. Conversely, renewable energy technology, including solar panels and wind turbines, which generate electricity from renewable sources, frequently introduces uncertainty and intermittency as a result of fluctuating environmental conditions. These unanticipated factors adversely affect the power system stability and reliability by causing voltage sags, swells, and flickers, thereby increasing the risk of equipment faults or failures. Consequently, the power system efficiency and performance are compromised, which requires advanced controllers and compensation techniques to ensure optimal power quality and a stable electricity supply to all connected loads. Therefore, a unified power quality conditioner (UPQC) is a comprehensive compensation technique introduced to address both current and voltage power quality problems. The integration of nonlinear loads and renewable energy equipment into a power system causes disturbances that exacerbate power quality issues on the load side. Consequently, enhancing UPQC performance is essential for addressing both anti-disturbance and power quality issues [1].

Current research on UPQC control strategies can be divided into three aspects, namely, the new compensation control strategy of UPQC [2–4], the UPQC topological structure [5,6], and the UPQC control strategy connected to renewable energy [7,8]. Artificial intelligence (AI) algorithms employed in the UPQC compensation control strategy have been designed to improve control accuracy by optimizing controller parameters. Nicola et al. [9] used the grey wolf algorithm to optimize the PI controller for reducing the steady-state error and DC ripple of the intermediate DC module to enhance the compensation performance of UPQC. Fuyin et al. [10] proposed a control method based on the beetle antenna search algorithm to optimize the parameters of the quasi-proportional integral resonant controller, hence improving the dynamic response speed and control accuracy of UPQC. Yadav et al. [11] employed a chicken flock algorithm to optimize the parameters of the fractional-order controller in the UPQC control system and minimize the THD value. Kumar et al. [12] proposed a minimum active power injection from UPQC to alleviate the imbalanced voltage sag caused by the voltage fluctuation at the grid side. The particle swarm algorithm has been mainly used to determine the optimal objective function of minimum active power injection. Zanib et al. [13] developed an artificial neural network controller to diminish the THD voltage at the load side by improving the dynamic and static performance of the UPQC control system. Such listed studies primarily focused on improving the UPQC control strategy by optimizing controller settings using AI algorithms. However, the goal function and system restrictions established during the optimization process may result in prolonged computational time. Furthermore, due to algorithmic limitations during the optimization process, these methods may become trapped in local optima.

On the other hand, current and voltage compensation of UPQC must be calculated based on the output angle of the detection link of the phase-lock loop (PLL). Kumar et al. [14] used the Jaya algorithm to optimize the gain of the proportional-integral (PI) controller for synchronous reference frame PLL (SRF-PLL) and dual second-order generalized integrator PLL (DSOGI-PLL), wherein the latter demonstrated superior mitigation of power quality problems through the use of UPQC. Bueno-Contreras et al. [15] designed a multi-input and output control strategy based on a resonant observer to reduce the coupling effect between UPQC and a grid system. Xu et al. [16] proposed a precise model of the second-order generalized integrator-based PLL (SOGI-PLL) based on the

absence of a feedback link in the PLL. This model fully considers the coupling of a frequency feedback loop and serves as a reference for the design of the PLL under non-ideal conditions in UPQC. In order to represent a dual second-order complex coefficient filter (DSOCCF) with DC offset rejection capability in UPQC, Hui et al. [17] focused on the detection requirements of grid synchronization signals under the mixed conditions of unbalance, harmonics, and DC voltage in conjunction with the moving average filter (MAF) method. In crucial situations, such as frequency variations, the suggested filter can swiftly and precisely identify the features of grid voltage. Li et al. [18] addressed the sub-synchronous resonance (SSR) problem induced by renewable energy connected to a weak grid system. The UPQC controller system uses an inertia PLL that effectively solves the SSR problem under a grid system; the Kalman filter with inherent adaptive bandwidth design uses the bat algorithm to optimize the PI gain controller to improve the PLL response speed and control accuracy required by the UPQC [19].

The abovementioned studies mostly focus on performance optimization and enhancing the design structure of PLLs utilized in UPQC. Still, there is a lack of studies on the performance of UPQC with PLL for cases that involve multiple disturbances. This research gap underlines the need for further investigations to improve the efficacy and adaptability of UPQC with PLL by accounting for various types of disturbances. The study will examine an innovative method of UPQC that improves anti-disturbance capabilities while reducing THD current and voltage on the load side. The proposed method focuses on enhancing the control strategy and PLL, which are the key components of UPQC. The UPQC utilization in a three-phase system with the three-wire system takes into account an enhanced control strategy using the finite control set-model predictive control (FCS-MPC), as well as a PLL optimized with a mixed second- and third-order generalized integer-based phase lock loop (MSTOGI-PLL) improved by linear active disturbance rejection control (LADRC). The FCS-MPC leverages a predictive model to optimize control strategies for reducing the error between the desired and actual values of current and voltage, resulting in lower THD. On the other hand, a conventional PLL is prone to poor dynamic response and phase errors, particularly in the presence of disturbances. Therefore, MSTOGI-PLL is utilized to improve synchronization and disturbance rejection, which will improve the UPQC performance. Moreover, the LADRC used in the MSTOGI-PLL block offers an extra layer of disturbance estimation and rejection, essential for compensating unknown or fluctuating disturbances in real-time, thereby enhancing the power quality issues addressed by UPQC while diminishing sensitivity to external disturbances.

This paper presents an improved UPQC control strategy that uses the FCS-MPC control system for a three-phase three-wire power system with UPQC compensation, and compares that with the traditional UPQC control strategy using a PI controller. An enhanced MSTOGI-PLL device utilizing LADRC is developed and evaluated against the PI-controlled SRF-PLL and the PI-controlled MSTOGI-PLL devices. The simulation results indicate that the UPQC control system enhanced by FCS-MPC significantly diminishes the harmonic THD values of the output current and voltage on the load side, while the phase-locked outcome of the refined MSTOGI-PLL device utilizing LADRC is more precise amidst various disturbances.

2. FCS-MPC control system with MOSTGI-PLL-based LADRC used in UPQC

A three-phase, three-wire power system with UPQC is depicted in Figure 1. It is made up of a shunt active power filter (APF) for current compensation and a series APF primarily for voltage compensation.

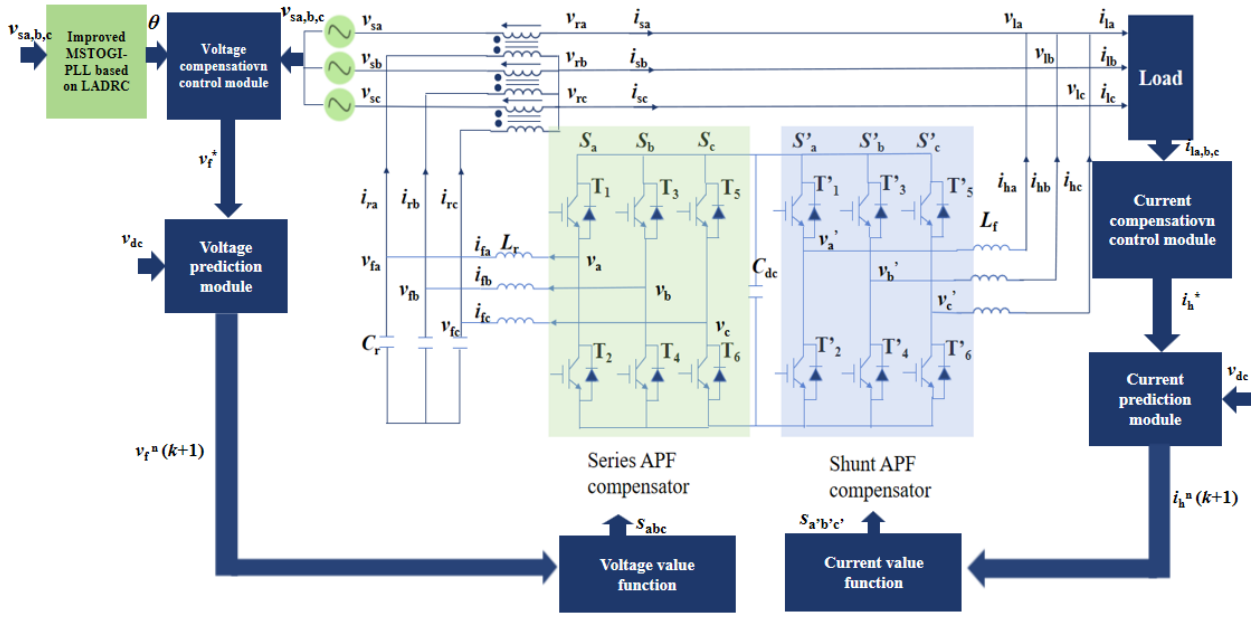


Figure 1. UPQC with FCS-MPC control system with MSTOGI-PLL-based LADRC.

In Figure 1, v_{sa}, v_{sb}, and v_{sc} are the three-phase voltages on the grid side; i_{sa}, i_{sb}, and i_{sc} are the three-phase currents on the grid side; v_{la}, v_{lb}, and v_{lc} are the three-phase voltages on the load side; i_{la}, i_{lb}, and i_{lc} are the three-phase currents on the load side; i_{ha}, i_{hb}, and i_{hc} are the compensation currents from the shunt APF; and v_{fa}, v_{fb}, and v_{fc} are the voltages on the series transformer connected with the converter of the series APF. Furthermore, C_r and L_r are the capacitor and inductor connected to the series APF, respectively; L_f is the inductor connected to the shunt APF; and C_{dc} is the intermediate DC capacitor.

After the grid voltages v_{sa}, v_{sb}, and v_{sc} are transmitted to the MSTOGI-PLL device, improved based on LADRC, the grid voltage angle estimation value θ is obtained. It is observed that the grid voltages $v_{sa,b,c}$ and the grid voltage angle estimation value θ of MSTOGI-PLL-based LADRC are transferred to the voltage compensation control module to generate the voltage reference, $v_f^*(k+1)$, required by the voltage prediction module to provide $v_f^n(k+1)$ for the voltage value function to transfer the optimal switching signals, S_{abc}, to the series APF compensator. The voltage prediction module inherently utilizes the FCS-MPC that provides the $v_f^n(k+1)$ so that the voltage value function will generate S_{abc} to the series APF compensator for improving the voltage conditions.

This is followed by the load-side current, i_{labc}, being transferred to the current compensation control module to generate the current reference, $i_h^*(k+1)$, required by the current prediction module for transferring the $i_h^n(k+1)$ to the current value function so that the optimal switch signals, $S_{a'b'c'}$, is received by the shunt APF compensator. The current prediction module inherently utilizes the FCS-MPC that provides the $i_h^n(k+1)$ so that the current value function will generate $S_{a'b'c'}$ to the shunt APF compensator for improving the current conditions.

3. UPQC using FCS-MPC connected to the series and shunt APF compensators

The FCS-MPC control method employed by UPQC compensates for voltage and current by discretizing the state equation to derive the projected values of voltage and current at time $k+1$. The

voltage and current value functions are established, and the voltage vector exhibiting the minimal deviation from the reference value is chosen via the selection of the value function. The switching signal for the chosen optimum voltage vector is subsequently applied to the IGBT device. The series APF and shunt APF use FCS-MPC technology to enable UPQC to select the optimal control vector to act on the system under the optimization of the value function when facing voltage surges, sags, and interruptions, thereby improving the compensation capacity of UPQC in three-phase three-wire power systems.

3.1. Integration of the voltage compensation control module and the voltage predictive control

The red dashed box of synchronous reference frame PLL (SRF-PLL) shown in Figure 2 uses the Clarke transformation in Equation (1) to convert the three-phase voltage $v_{sa,b,c}$ on the grid side into $v_{s\alpha,\beta}$ in the αβ coordinate system.

$$\begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \\ v_{s0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{1}$$

Additionally, the $v_{s\alpha}$ and $v_{s\beta}$ are transformed using Park transformation, as described in Eq (2), resulting in v_{sq} inside the dq coordinate system, which serves as the input parameter for the PI controller. Subsequently, the grid voltage angle estimation, θ, is derived through integral remainder computation. This is related to the SRF-PLL, which is employed to calculate the output angle θ for voltage and current correction or compensation. The grid voltage values in the dq coordinate system, following Park translation, are denoted as v_{sd} and v_{sq}, as specified in Eq (2).

$$\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} \tag{2}$$

In the red dashed box of the voltage compensation control module, the grid voltage amplitude of v_s is multiplied by the θ under sine and cosine, which is negatively fed back to $v_{s\alpha}$ and $v_{s\beta}$ to obtain the values of $v_{s\alpha,h}$ and $v_{s\beta,h}$. Simultaneously, $v_{s\alpha,h}$ and $v_{s\beta,h}$ are used in Eq (1) to allow the Clarke transformation to produce the $v_{sa,h}$, $v_{sb,h}$, and $v_{sc,h}$ that represent the $v_f^*(k+1)$ required by the voltage prediction module, as shown in Figures 1 and 2. The $v_f^*(k+1)$, consisting of $v_{sa,h}$, $v_{sb,h}$, and $v_{sc,h}$, will be used in the voltage value function to compare with the $v_f^n(k+1)$ computed by the voltage prediction module. The voltage prediction module that produced the $v_f^n(k+1)$ is derived based on the following discussion.

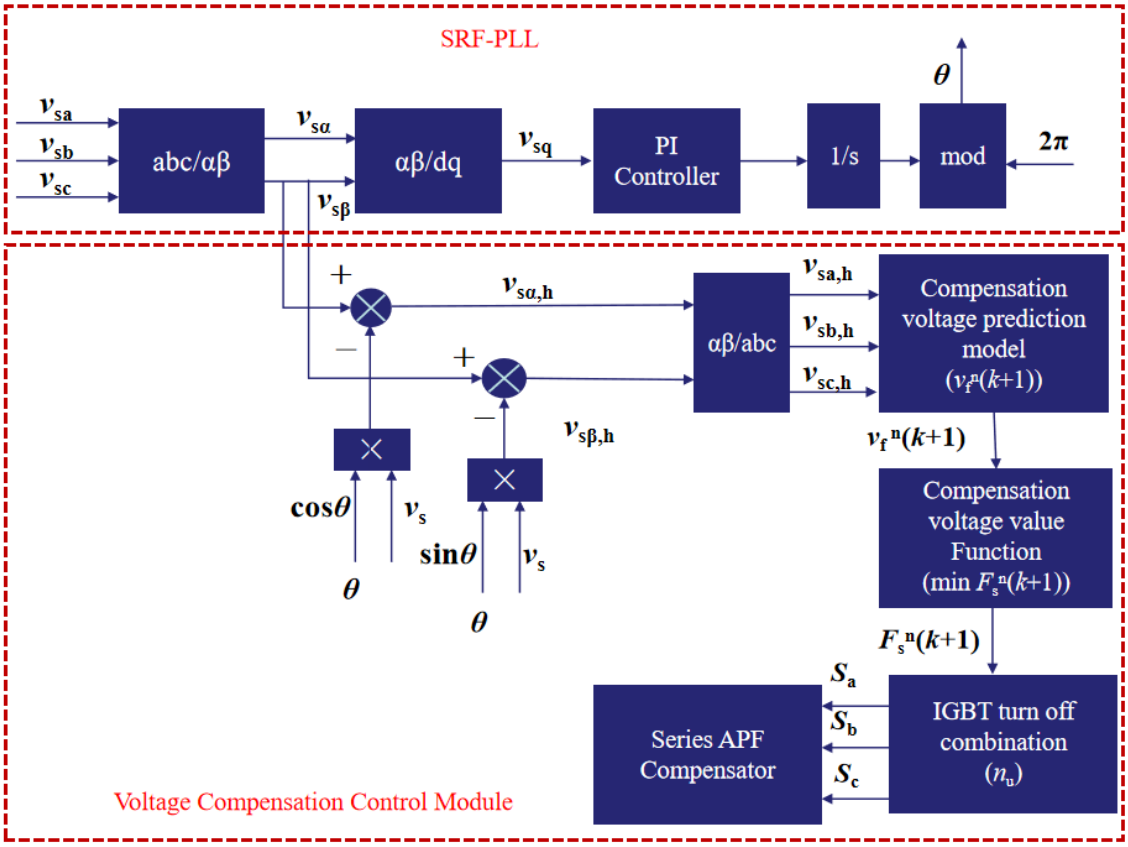


Figure 2. Principle diagram of the voltage compensation control module and the voltage prediction module.

The voltage prediction module output of $v_f^n(k+1)$ is derived based on the concept of the grid voltage compensation circuit at the series APF compensator of the UPQC shown in Figure 1. Equation (3) is derived from the concept of balanced equivalent circuits, referring to the grid voltage compensation circuit of the series APF compensator.

$$L_r \frac{di_{fa,b,c}}{dt} = v_{a,b,c} - v_{fa,b,c} \tag{3}$$

where L_r is the inductance of the grid voltage compensation circuit at the series APF compensator; $i_{fa,b,c}$ are the inductance currents; $v_{fa,b,c}$ are the voltage drops of capacitors C_r, and $v_{a,b,c}$ are the node voltages at the bridge arm IGBTs of the series APF compensator.

In Eq (4), the concept of balanced equivalent circuits is utilized by referring to the grid voltage compensation circuit of a series APF compensator.

$$C_r \frac{dv_{fa,b,c}}{dt} = i_{fa,b,c} - i_{ra,b,c} \tag{4}$$

where $i_{ra,b,c}$ are the secondary currents of the series transformer.

On the other side, the output voltage of inverters, $v_{a,b,c}$, refers to the switching state of the upper and lower bridge arms of IGBTs. Therefore, the voltage vector $\dot{v}$ is based on the finite control set (FCS) that can be written as in Eq (5).

$$\dot{v} = v_{a,b,c} = \frac{2}{3} v_{\mathrm{dc}} (\mathrm{S_a} + a\mathrm{S_b} + a^2 S_\mathrm{c}) \tag{5}$$

where $a = \mathrm{e}^{\mathrm{j}(2\pi/3)}$, and v_{dc} is a DC-link voltage connected with a capacitor C_r. The switching state for the bridge arm IGBTs is given in Eq (6).

$$S_\mathrm{k} = \begin{cases} 0 \\ 1 \end{cases}, \quad k = \mathrm{a,b,c} \tag{6}$$

In Eq (6), $S_\mathrm{k} = 0$ means the upper bridge arm IGBT is turned off, and the lower bridge arm IGBT is turned on. Additionally, $S_\mathrm{k} = 1$ means the upper bridge arm IGBT is turned on, and the lower bridge arm IGBT is turned off. Therefore, S_a, S_b, and S_c are arranged in eight different switching states, yielding eight voltage vectors $\dot{v}$.

By integrating Eqs (3) and (4), the state equation is obtained, as shown in Eq (7).

$$\frac{\mathrm{d}\dot{x}}{\mathrm{d}t} = \mathrm{A}\dot{x} + \mathrm{B}\dot{v} + \mathrm{C}\dot{i}_\mathrm{r} \tag{7}$$

where, $\mathrm{A} = \begin{bmatrix} 0 & -\frac{1}{L_\mathrm{r}} \\ \frac{1}{C_\mathrm{r}} & 0 \end{bmatrix}$; $\mathrm{B} = \begin{bmatrix} \frac{1}{L_\mathrm{r}} \\ 0 \end{bmatrix}$; $\mathrm{C} = \begin{bmatrix} 0 \\ -\frac{1}{C_\mathrm{r}} \end{bmatrix}$; $\dot{x} = \begin{bmatrix} i_{\mathrm{fa,fb,fc}} \\ v_{\mathrm{fa,fb,fc}} \end{bmatrix}$; $\dot{v} = [v_\mathrm{a}, v_\mathrm{b}, v_\mathrm{c}]$; $\dot{i}_r = [i_\mathrm{ra}, i_\mathrm{rb}, i_\mathrm{rc}]$

Consequently, Equation (8) is obtained by performing forward Euler discretization on Eq (7).

$$\dot{x}(k+1) = \mathrm{A}_1 \dot{x}(k) + \mathrm{B}_1 \dot{v}(k) + \mathrm{C}_1 \dot{i}_\mathrm{r}(k), \tag{8}$$

where $\mathrm{A}_1 = \begin{bmatrix} a_1 & a_2 \\ a_3 & a_4 \end{bmatrix} = \begin{bmatrix} \cos\omega_0 T & -\frac{1}{\omega_0 L_\mathrm{r}} \sin\omega_0 T \\ \frac{1}{\omega_0 C_\mathrm{r}} \sin\omega_0 T & \cos\omega_0 T \end{bmatrix}$; $\mathrm{B}_1 = \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} \frac{1}{\omega_0 L_\mathrm{r}} \sin\omega_0 T \\ 1 - \cos\omega_0 T \end{bmatrix}$;

$\mathrm{C}_1 = \begin{bmatrix} c_1 \\ c_2 \end{bmatrix} = \begin{bmatrix} 1 - \cos\omega_0 T \\ -\frac{\sin\omega_0 T}{\omega_0 C_\mathrm{r}} \end{bmatrix}$; $\omega_0 = \frac{1}{\sqrt{L_\mathrm{r} C_\mathrm{r}}}$; T represents the period value.

Finally, the model predictive control (MPC) voltage of $v_\mathrm{f}^n(k+1)$ at time $k+1$ is derived as follows:

$$v_\mathrm{f}^n(k+1) = a_3 i_\mathrm{f}(k) + a_4 v_\mathrm{f}(k) + b_2 \dot{v}_\mathrm{n}(k) + c_2 \dot{i}_\mathrm{r}(k) \tag{9}$$

where n is the state number of 0, 1, 2, ..., and 7.

Simultaneously, the voltage value function, $F_\mathrm{s}^n(k+1)$, is performed to compare the recently obtained $v_\mathrm{f}^n(k+1)$ with the $v_\mathrm{f}^*(k+1)$ provided by the voltage compensation control module discussed earlier in this subsection. Hence, the minimum voltage value function, min $F_s^n(k+1)$, of Eq (10) is used as a reference to select the optimal switching state, $\hat{S}_k$, for turning on and off the bridge arm IGBTs in every phase at time $k+1$, as shown in Eq (11).

$$\min\ F_s^n(k+1) = \left\| v_f^*(k+1) - v_f^n(k+1) \right\|^2 \tag{10}$$

$$\hat{S}_k \approx \min\ F_s^n(k+1) \tag{11}$$

The $\hat{S}_k$ will reduce the compensation voltage pulsation during the switching of bridge arm IGBTs located at the series APF compensator of UPQC.

3.2 Integration of the current compensation control module and the current predictive control

Figure 3 illustrates the current compensation control module highlighted by the red dashed box. The Clarke transformation in Eq (1) is used to convert the load currents, i_{la}, i_{lb}, and i_{lc}, becoming $i_{l\alpha}$ and $i_{l\beta}$ in the αβ coordinate system. This is followed by the Park transformation in Eq (2) that is used to determine the i_{ld} in the dq system that refers to the input information of $i_{l\alpha}$ and $i_{l\beta}$. The low-pass filter filtering output, the DC control module output, and the PLL output angle, θ, are considered to determine the $i_{l\alpha,h}$ and $i_{l\beta,h}$ in the αβ coordinate system so that the Clarke transformation in Eq (1) will produce $i_{la,h}$, $i_{lb,h}$, and $i_{lc,h}$, representing the $i_h^*(k+1)$ required by the voltage prediction module, as shown in Figures 1 and 3. The $i_h^*(k+1)$, comprising $i_{la,h}$, $i_{lb,h}$, and $i_{lc,h}$, is used by the current value function to compare with the $i_h^n(k+1)$ calculated by the current prediction module. The next clarification will detail the derivation of $i_h^n(k+1)$ generated by the present prediction module.

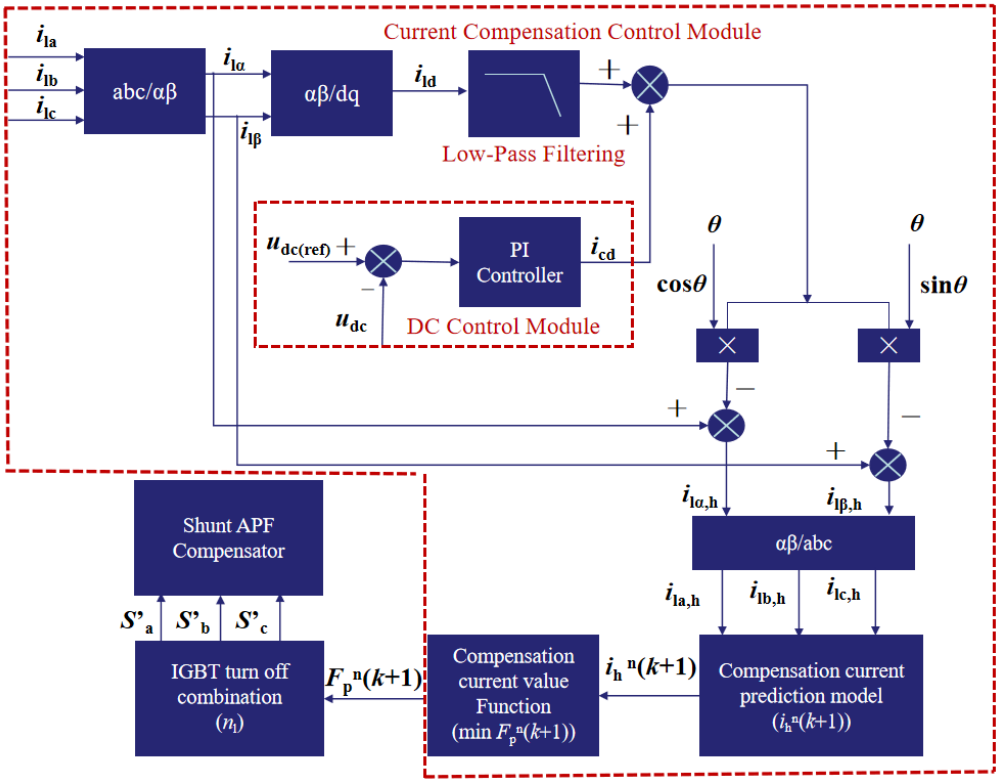


Figure 3. Principle diagram of the current compensation control module and current prediction module.

The current prediction module output of $i_h^n(k+1)$ is derived based on the concept of a grid current compensation circuit connected to the shunt APF compensator of the UPQC shown in Figure 1. The concept of balanced equivalent circuits is used to derive Eq (12); it refers to the grid current compensation connected at the shunt APF compensator of the UPQC depicted in Figure 1.

$$L_f \frac{di_{ha,b,c}}{dt} = v'_{a,b,c} - v_{la,b,c} \tag{12}$$

where L_f is the inductance of the grid current compensation circuit at the shunt APF compensator; $v_{la,b,c}$ are the load voltages; and $v'_{a,b,c}$ are the node voltages at the bridge arm IGBTs of the shunt APF compensator.

By abbreviating the variables in Eqs (12), Eq (13) is obtained, representing the balanced equivalent circuits for the grid current compensation connected to the shunt APF compensator of the UPQC.

$$L_f \frac{d\dot{i}_h}{dt} = v' - v_l \tag{13}$$

By performing forward Euler discretization on Eq (13), the model predictive control (MPC) current of $i_h^n(k+1)$ at time $k+1$ is obtained, as shown in Eq (14).

$$i_h^n(k+1) = i_h(k) + \frac{T}{L_f} v'_n(k) - \frac{T}{L_f} v_l(k) \tag{14}$$

Therefore, the voltage vector, $v'_n(k)$, is calculated based on the concept of FCS using Eq (5) and represents the v'_a, v'_b, and v'_c at the bridge arm IGBTs, shown in Figure 1.

Consequently, the current value function, $F_p^n(k+1)$, is carried out for comparing between the $i_h^n(k+1)$ and $i_h^*(k+1)$ provided previously by the current compensation control module. Eventually, Equation (15) gives the minimum current value function, min F_p^n(k+1), that is used as a reference in Eq (16) to select the optimal switching state, $\hat{S}_k$, with the goal of minimizing compensation voltage pulsation during the switching of bridge arm IGBTs in every phase at time $k+1$ for the shunt APF compensator of the UPQC.

$$\min F_p^n(k+1) = \left\| i_h^*(k+1) - i_h^n(k+1) \right\|^2 \tag{15}$$

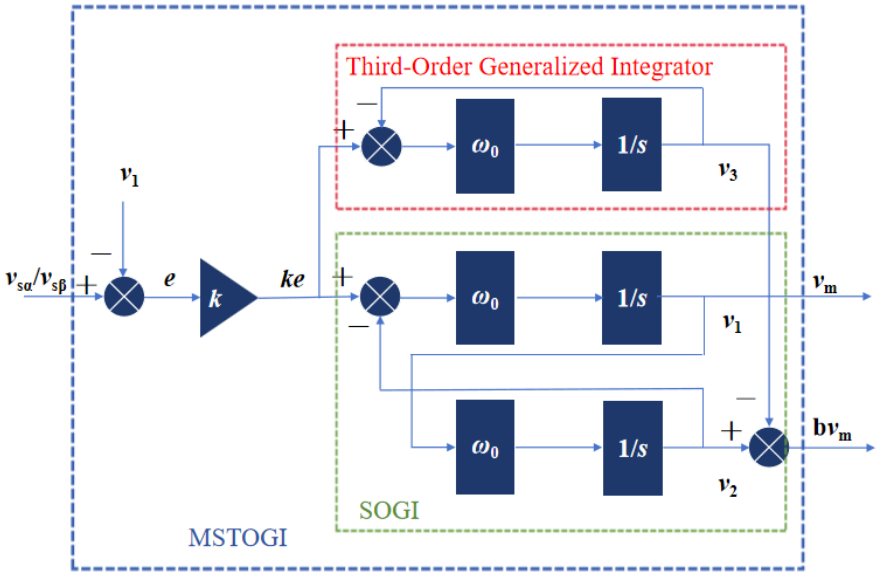
$$S'_k \approx \min F_p^n(k+1) \qquad k=a,b,c \tag{16}$$

4. MSTOGI-PLL-based LADRC in the series and shunt APF of UPQC

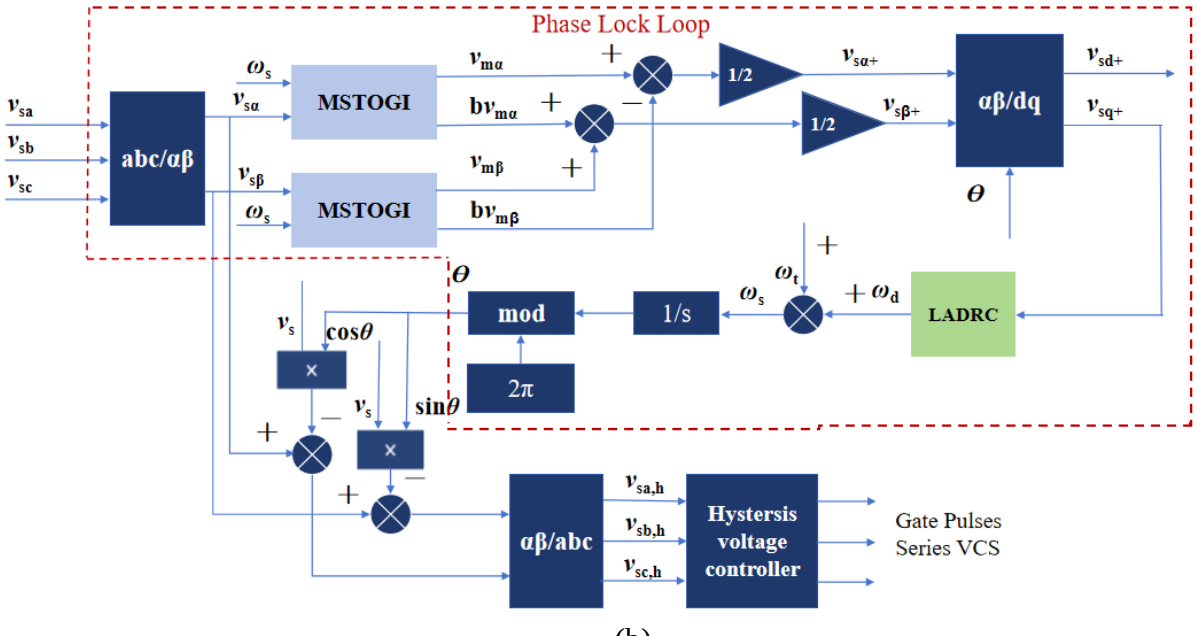
The SRF-PLL output result in Figure 2 is prone to disturbances, which eventually deteriorate the compensation effect of UPQC. A novel mixed second- and third-order generalized integrator PLL (MSTOGI-PLL)-based linear anti-disturbance rejection controller (LADRC) enhancement is introduced to replace the SRF-PLL to improve the response speed and anti-disturbance capabilities of the PLL under different power quality problems, such as voltage sag, voltage swell, and harmonics. Particularly, two MSTOGIs are considered in the PLL, which is then integrated with the LADRC.

4.1. Design model of MSTOGI-PLL-based LADRC

The MSTOGI is an improved version of PLL used to address the shortcomings of the second-order generalized integrator (SOGI) in terms of its sensitivity to frequency variations and its quality factor changes corresponding to the input signal frequency. The high-frequency component is suppressed, and the DC components are efficiently filtered out in Figure 4(a) using the MSTOGI-PLL. As a result, MSTOGI-PLL has advantageous output characteristics in both high- and low-frequency bands that improve the system's dynamic reaction time, address detection delay problems, and confirm detection accuracy. Two MSTOGIs incorporated into the PLL and connected to the LADRC are shown by the red dotted box in Figure 4(b).



(a)



(b)

Figure 4. (a) Design model of MSTOGI; (b) MSTOGI-PLL integrated with LADRC.

Three branches of v_1, v_2, and v_3 build the structure of the MSTOGI model, as shown in Figure 4(a). The error signal, e, is amplified by gain k to obtain a new error signal, ke. The output of v_1 is an AC-containing signal that is in phase with $v_{s\alpha}$ and $v_{s\beta}$ originating from a Clarke transformation of grid voltage supply v_{sa}, v_{sb}, and v_{sc}, as shown in Figure 4(b). The output signal of v_2 consists of DC and AC components. The AC component has the same amplitude and frequency as the output signal of v_1, and its phase lags behind v_1 by 90 °. The DC components are the same for both output signals of v_2 and v_3.

By referring to Figure 4(b), an unbalanced disturbance in a power system can usually be detected by using the symmetrical component method by decomposing the voltage and current into positive sequence, negative sequence, and zero sequence quantities. The symmetrical component method used in the detection process is shown in Eq (17).

$$\begin{bmatrix} v_{sa+} \\ v_{sb+} \\ v_{sc+} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix}\begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{17}$$

In Eq (17), v_{sa+}, v_{sb+}, and v_{sc+} are the positive sequence component values of the three-phase voltage on the grid side, and a is the 120 ° angle phase operator. Then, the positive sequence three-phase component is transformed into the αβ coordinate system by using the Park transformation of Eq (18). The $v_{s\alpha+}$ and $v_{s\beta+}$ are the positive sequence components of the voltage on the grid side in the αβ coordinate system.

$$\begin{bmatrix} v_{s\alpha+} \\ v_{s\beta+} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_{sa+} \\ v_{sb+} \\ v_{sc+} \end{bmatrix} \tag{18}$$

Equation (19) is obtained by substituting Eq (17) into Eq (18) and performing a Clarke inverse transformation. In Eq (19), b is the time domain phase shift operator, whose function is to convert the positive sequence signal of the grid voltage into two mutually orthogonal quantities.

$$\begin{bmatrix} v_{s\alpha+} \\ v_{s\beta+} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 & -b \\ b & 1 \end{bmatrix}\begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} \tag{19}$$

In Figure 4(a), v_3 in the dotted box is a module for eliminating the DC component. The DC component is eliminated by subtracting v_3 from v_2. Hence, the v_m and bv_m are obtained as two mutually orthogonal voltage outputs. ω_0 is the resonant frequency of MSTOGI. Assume that the frequency of the input signal v is ω_s. Since $\omega_0 = \omega_s$, v_1 does not contain the DC component, and the AC component is the same as the input signal v. The specific elimination of the DC component is shown in Eqs (20) and (21).

$$v_m = v_1 \tag{20}$$

$$bv_m = v_2 - v_3 \tag{21}$$

In Figure 4(b), ωt is a variable value mainly used to speed up the detection speed of the PLL. If this value is not introduced, the detection speed of the PLL can only be accelerated by adjusting the PI controller. However, this approach will produce a large overshoot and increase the instability of the control system. Subsequent to empirical testing, this study sets ωt as the value of 100π. The values of fundamental positive sequence components of $v_{s\alpha+}$ and $v_{s\beta+}$ extracted from the grid side are shown in Eqs (22) and (23), similar to Eq (18).

$$v_{s\alpha+} = \frac{1}{2}(v_{m\alpha} - bv_{m\beta}) \tag{22}$$

$$v_{s\beta+} = \frac{1}{2}(bv_{m\alpha} + v_{m\beta}) \tag{23}$$

The voltage values of $v_{s\alpha+}$ and $v_{s\beta+}$ in the dq coordinate system are transformed by the Park formulation given in Eq (2), so that the v_{sq+} can be used by the LADRC to improve the θ. Then, the $v_{s\alpha+}$, $v_{s\beta+}$, and θ are used in the voltage compensation control module in Figure 2 to compensate for the unknown or varying disturbances in a real-time manner with fast dynamic response and minimum phase errors for better synchronization during the mitigation of power quality problems.

4.2. LADRC controller model

It is worthwhile to mention that the first-order LADRC, used to replace the PI in the MSTOGI-PLL, is responsible for improving the poor anti-disturbance ability, as shown in Figure 4(b). Figure 5 shows a detailed circuit of the first-order LADRC model normalized by the amplitude normalization scheme (ANS) $v_{sq+} = \sqrt{\left(v_{sq+}^2 + v_{sd+}^2\right)}$, in order to ensure a robust performance of the MSTOGI-PLL at the grid connection point. The feedback value for the fundamental positive sequence component of q-axis voltage, v_{sq+}, can be written as a differential equation in Eq (24).

$$\frac{\mathrm{d}v_{sq+}}{\mathrm{d}t} = -\omega_{\mathrm{d}} + \Delta\omega + \frac{\mathrm{d}\tilde{u}_{\mathrm{q}}}{\mathrm{d}t} + d_{\mathrm{x}} \tag{24}$$

where ω_{d} is the input of LADRC, $\triangle\omega$ represents the disturbance caused by the frequency and phase angle changes, $\tilde{u}_{\mathrm{q}}$ represents the disturbance caused by the negative sequence and background harmonics, and d_{x} is the other external disturbances in the unmodeled dynamic and grid-connected point voltage signal. Equation (24) is simplified, becoming Eq (25), which allows the controlled object $u = -\omega_{\mathrm{d}}$, and the total system disturbance is $f = \nabla\omega + \frac{\mathrm{d}\tilde{u}_{\mathrm{q}}}{\mathrm{d}t} + d_{\mathrm{x}}$.

$$\frac{\mathrm{d}v_{sq+}}{\mathrm{d}t} = u + f \tag{25}$$

Equation (25) shows that the first-order PLL considers different types of disturbance. The first-order LADRC that is used to improve the control stability of the system is comprised of three primary components, which are the linear tracking differentiator (LTD), linear state error feedback rate (LSEF), and linear extended state observer (LESO). Since $v_{sq+(ref)}$ is set to 0 as a reference value,

the LTD tracking signal is not required by the LADRC. Therefore, Equation (26) is the state space equation derived from Eq (25).

$$\begin{bmatrix} \dot{v}_{sq+} \\ \dot{f} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{sq+} \\ f \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} u \\ F \end{bmatrix} \tag{26}$$

$$y = v_{sq+} \tag{27}$$

where F is the differential of the total disturbance f, y is the system output, and u is the system input. Equation (28) illustrates the LESO formulation derived by referring to Eqs (26) and (27).

$$\begin{bmatrix} \dot{z}_1 \\ \dot{z}_2 \end{bmatrix} = \begin{bmatrix} -\beta_1 & 1 \\ -\beta_2 & 0 \end{bmatrix} \begin{bmatrix} z_1 \\ z_2 \end{bmatrix} + \begin{bmatrix} b_0 & \beta_1 \\ 0 & \beta_2 \end{bmatrix} \begin{bmatrix} u \\ y \end{bmatrix} \tag{28}$$

where z_1 is the estimated value of v_{sq+}, z_2 is the estimated value of the total disturbance f, b_0 is the adjustable gain of the system, and the specific construction of LSEF is given as follows:

$$u = -\omega_d = \frac{G(v_{sq+(ref)} - z_1) - z_2}{b_0} \tag{29}$$

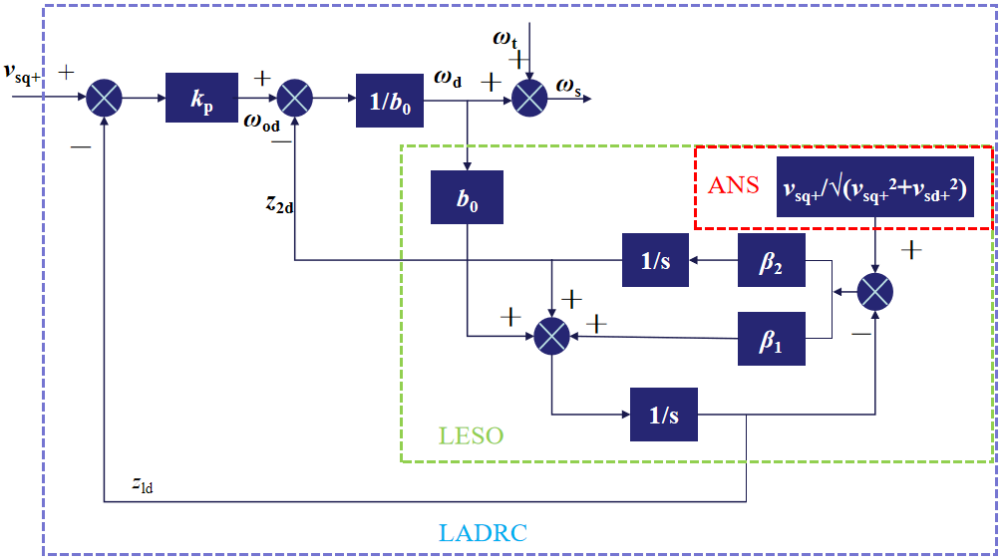


Figure 5. LADRC circuit model.

where G is the feedback gain coefficient. Equations (26) to (29) are simplified as a two-degree-of-freedom system represented by $C_1(s)$ and $C_2(s)$, as written in Eqs (30) and (31).

$$C_1(s) = \frac{(\beta_1 G + \beta_2)s + \beta_2 G}{b_0 s(s + \beta_1 + G)} \tag{30}$$

$$C_2(s) = \frac{G(s^2 + \beta_1 s + \beta_2)}{(\beta_1 G + \beta_2)s + \beta_2 G} \tag{31}$$

In Eqs (30) and (31), the primary role of C_2(s) is to pre-filter the input signal in the form of a first-order differential. $C_2(s)$ is not considered in the analysis since the $v_{sq+(ref)}$ is set as 0. Figure 6 shows the two-degree-of-freedom control system for Eqs (30) and (31).

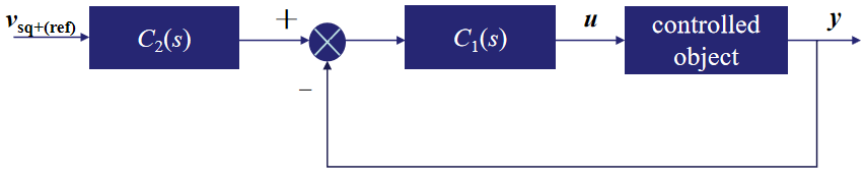


Figure 6. The two-degree-of-freedom control system of LADRC.

In Eq (30), C_1(s) represents a PI controller combined with a low-order filter that can also be written as in Eq (32).

$$C_1(s) = \frac{(\beta_1 G + \beta_2) + \beta_2 G}{b_0 s(s + \beta_1 + G)} = \frac{k_p s + k_i}{s} \cdot \frac{\omega_p}{s + \omega_p} = \frac{k_p \cdot \omega_p (s + \omega_z)}{s(s + \omega_p)} \tag{32}$$

where k_i is the integral coefficient of the corresponding PI controller, k_p is the proportional coefficient, which is also the bandwidth coefficient of the controller, ω_p is the bandwidth of the corresponding first-order low-pass filter, and ω_z is the ratio of the integral coefficients. The coefficients are given in Eqs (33)–(36).

$$k_p = \frac{\beta_1 G + \beta_2}{b_0(\beta_1 + G)} \tag{33}$$

$$k_i = \frac{\beta_2 G}{b_0(\beta_1 + G)} \tag{34}$$

$$\omega_p = \beta_1 + G \tag{35}$$

$$\omega_z = \frac{k_i}{k_p} \tag{36}$$

In Eqs (33)–(35), the reference bandwidth method uses a unified observation bandwidth ω_0 to adjust β_1 and β_2, as shown in Eqs (37) and (38).

$$\beta_1 = 2\omega_0 \tag{37}$$

$$\beta_2 = \omega_0^2 \tag{38}$$

The LADRC parameters of G and b_0 can be obtained using Eqs (33) and (34) with the proportional and integral parameters k_p, k_i, and the suitable ω_0 value provided by the PI controller.

As can be seen from the above derivation, the main parameter ω_0 of the observer bandwidth can determine the value of β_1 and β_2, which can be obtained by Eqs (37) and (38). The controller bandwidth k_p is usually obtained by empirical formulas, as shown in Eq (39).

$$k_p = (1/5 \sim 1/2)\omega_0 \tag{39}$$

5. Results and discussion

The Matlab/Simulink module is used to design the UPQC circuit using an FCS-MPC control system with the MSTOGI-PLL based on the LADRC, as shown in Figure 1. The key parameters employed in the power system connected with the UPQC are listed below. In the simulation, two main types of controllers are used for phase-locked loops: LADRC controllers and PI controllers. In the LADRC controller, $b_0 = 1$, $k_p = 48$, and $\omega_0 = 48$; in the PI controller, $P = 0.06$, and $I = 1.2$.

Table 1. Specific parameters used in the UPQC system**.**

Parameters	Values
Grid side voltage v_s	380 V
Grid side voltage frequency	50 Hz
L_r	5 mH
C_r	88 uF
L_f	5 mH
C_{dc}	10 uF
*L*oad(*R-L*)	2 Ω -8 mH

In Case I, the UPQC only compares the PLL with other controllers, which are the MSTOGI-PLL with the PI controller, the MSTOGI-PLL with the LADRC controller, and the SRF-PLL with the PI conventional controller. The performance of three different voltage compensation module PLLs used in UPQC is compared to investigate the accuracy and response time of the output angle θ under the same voltage disturbances at the grid-side power supply shown in Figure 7. The specific disturbance changes of the grid-side voltage v_{sabc} are shown in Table 2.

Table 2. Specific disturbances in grid-side voltage v_{sabc}.

Time period	v_{sabc} specific value
0–0.2 s	380 V
0.2–0.3 s	0.15*380 V
0.3–0.4 s	1.15*380 V
0.4–0.5 s	0.6*380 V
0.5–0.7 s	0 V
0.7–1 s	1.5*380 V

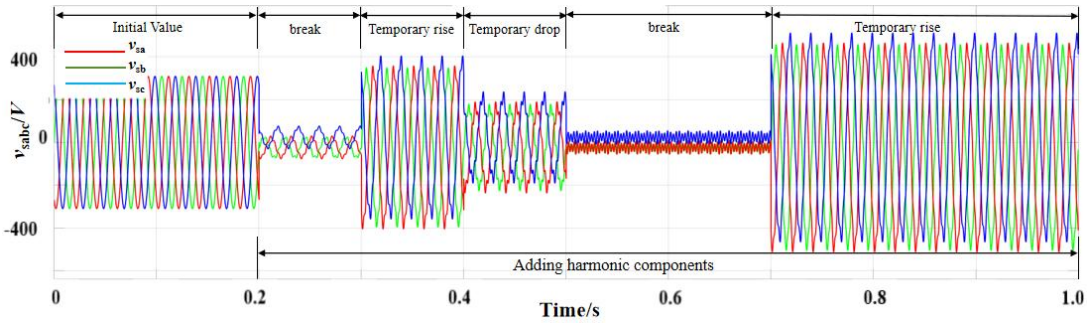


Figure 7. Grid voltage disturbances waveform for Case I.

In Figure 8, the red, blue, and green waveforms are the angle waveform outputs of θ provided by the MSTOGI-PLL with LADRC, MSTOGI-PLL with PI, and SRF-PLL with PI controllers, respectively, that are used in UPQC to perform the compensation of significant grid voltage drop or interruption during the time duration of 0.5–0.7 s, as shown in Figure 7. The SRF-PLL with PI and MSTOGI-PLL with LADRC controllers are shown in Figures 2 and 5, respectively. In reference to Figure 5, the MSTOGI-PLL with PI controllers is constructed by replacing the LADRC with PI. Figure 8 shows that the MSTOGI-PLL with LADRC controller has the fastest response time in compensating grid voltage disturbances, while the MSTOGI-PLL with PI controller has the second fastest response time due to the θ delay. The SRF-PLL using the PI controller is adversely affected by the grid voltage interruption. During this time interval, the controller no longer provides accurate phase-locked results due to indistinct information from a small oscillating θ waveform.

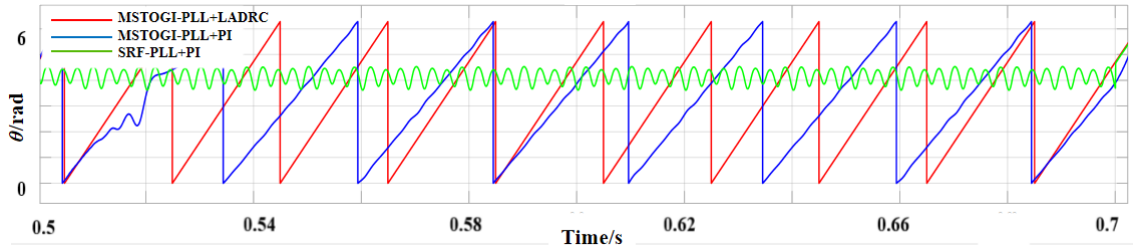


Figure 8. Phase-locked angle θ waveforms for the three PLL controller devices within the 0.5–0.7 s time period of significant grid voltage drop or interruption.

In Figure 9, the red, blue, and green waveforms are the v_{sd+} obtained from the MSTOGI-PLL with LADRC, MSTOGI-PLL with PI, and SRF-PLL with PI used in UPQC, respectively. The results of v_{sd+} show that the SRF-PLL with PI has the fastest response time and the smallest overshoot during the period of 0–0.2 s. On the other hand, the MSTOGI-PLL with LADRC has a slower response time of v_{sd+} than the SRF-PLL with PI during the initial period of 0–0.2 s. The MSTOGI-PLL with PI has a large overshoot during the starting time, followed by a slow response time, as well as an unstable slanted waveform of v_{sd+} during the period 0–0.2 s. On the other hand, harmonic disturbances were added to the grid voltage during a 0.2–1 s time period, resulting in noticeable v_{sd+} oscillations produced by the SRF-PLL with PI.

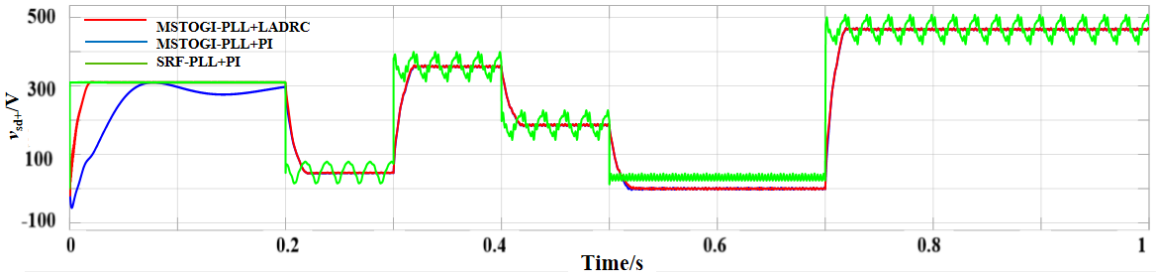


Figure 9. Output v_{sd+} waveforms of three-phase-locked devices within the period of 0–1 s.

Case II focuses on applying three-phase-locked devices of MSTOGI-PLL with LADRC, MSTOGI-PLL with PI, and SRF-PLL with PI controllers to the three-phase three-wire power system with UPQC compensation in the FCS-MPC system. The UPQC adopts the three-phase-locked devices operating under two different linear controllers, and several interruptions are applied, causing grid voltage waveform variations of v_{sabc}, as shown in Figure 10. The specific voltage values of the grid-side voltage v_{sabc} are shown in Table 3. The two linear controllers are performed by LADRC or PI. The result signifies that the PI controller with SRF-PLL is insufficient for effective grid voltage compensation in UPQC, while the LADRC controller with the MSTOGI-PLL device is the best phase-locked device for effective grid voltage compensation in UPQC.

Table 3. Specific disturbances in grid-side voltage v_{sabc}.

Time period	v_{sabc} specific value
0–0.1 s	380 V
0.1–0.25 s	0.85*380 V
0.25–0.5 s	380 V
0.5–0.6 s	1.15*380 V
0.6–0.7 s	380 V
0.7–0.75 s	0 V
0.75–1 s	380 V

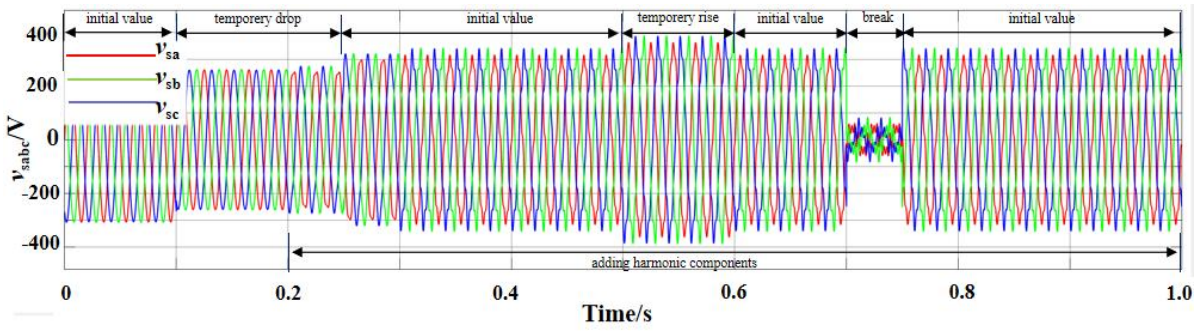


Figure 10. Distortions of the grid voltage waveform, v_{sabc}, occurring in the system.

Figures 11(a) and (b) show that the load currents of i_{la} in phase A are fairly constant under UPQC with linear control applied in the MSTOGI-PLL with LADRC and MSTOGI-PLL with PI, respectively. This refers to the grid voltage interruptions, v_{sabc}, applied from the incoming source or generator of the system shown in Figure 10. However, the UPQC with the linear control of SRF-PLL

with PI fails to effectively compensate for the load current, presenting high distortion of the i_{la} waveform during grid voltage interruption at 0.7–0.75 s.

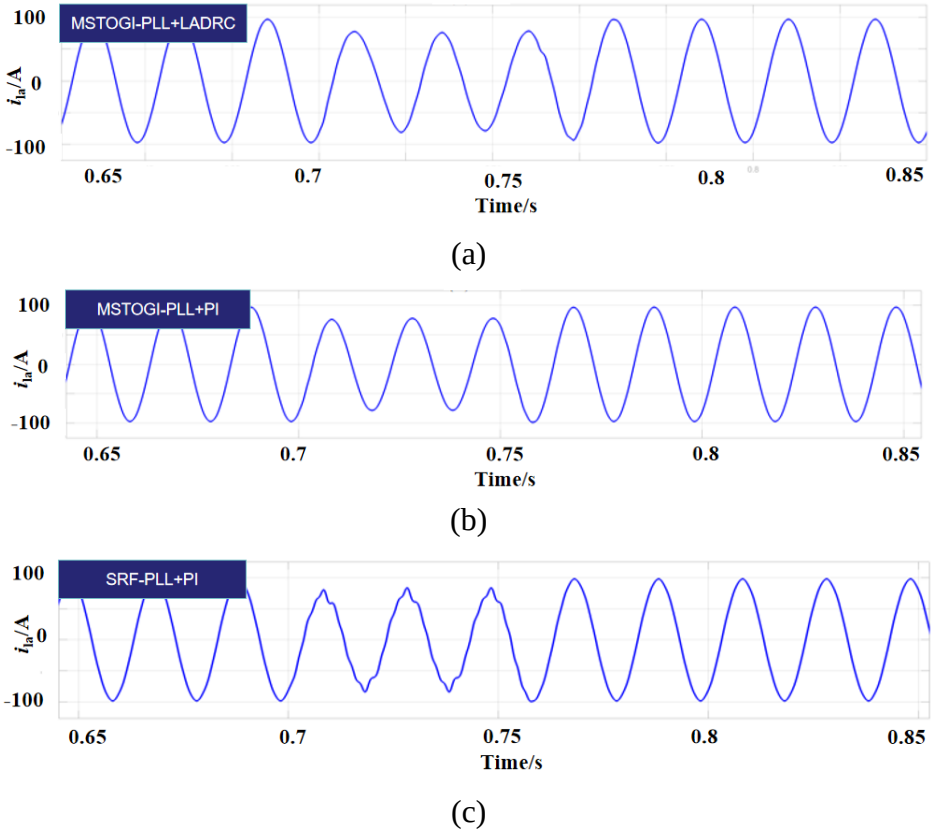


Figure 11. Load current waveforms of i_{la} under the phase-locked device of (a) MSTOGI-PLL with LADRC, (b) MSTOGI-PLL with PI, and (c) SRP-PLL with PI.

Figures 12(a), (b), and (c) show the load voltage of phase A, v_{la}, compensated by the three-phase-locked devices operating under linear control during the grid voltage interruptions that occurred within the time frame of 0.6–0.75 s, as depicted in Figure 7. During this case of grid voltage interruptions, the phase-locked devices of MSTOGI-PLL with LADRC and MSTOGI-PLL with PI yield the least deformation or distortion of the load voltage waveform, v_{la}, in contrast to the SRF-PLL with PI. In conjunction with the ineffective operation of SRF-PLL with PI, the v_{la} waveform distortion is obvious during a significant voltage interruption caused by the generator breaking throughout the period of 0.7–0.75 s.

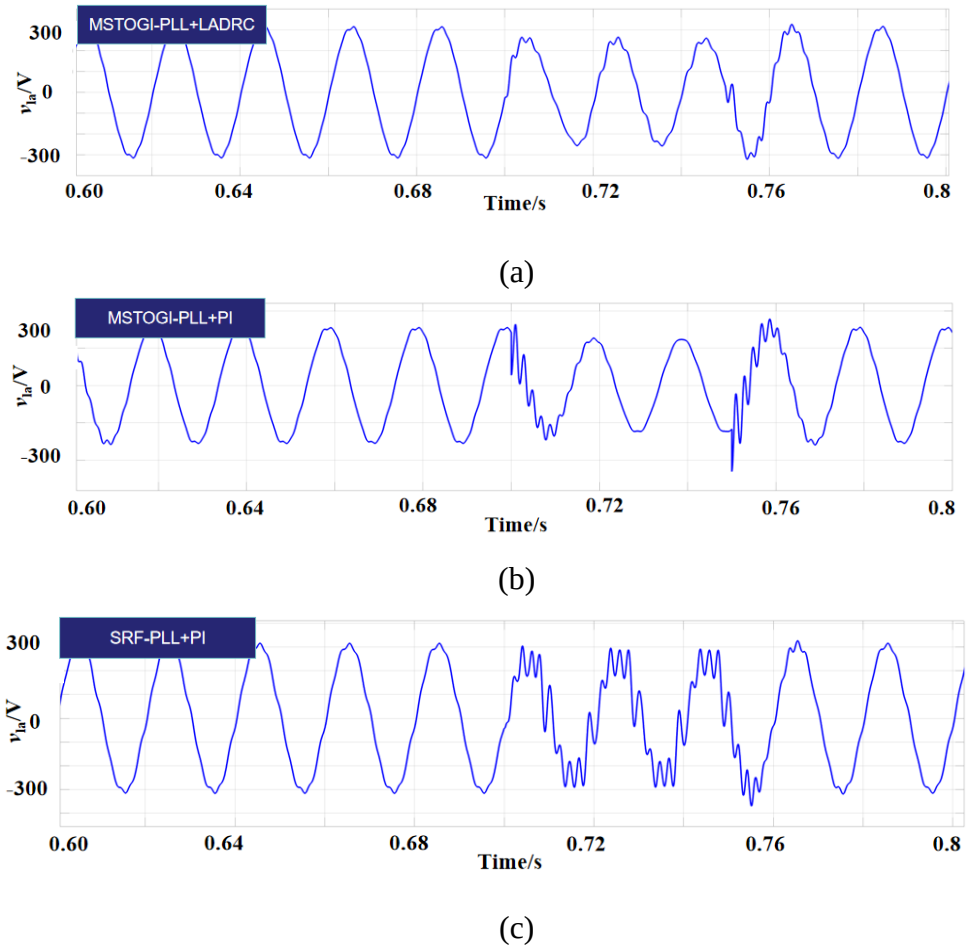


Figure 12. Load voltage waveforms of v_{la} within 0.6–0.8 s compensated by (a) the MSTOGI-PLL with LADRC, (b) the MSTOGI-PLL with PI, and (c) the SRF-PLL with PI.

Case III examines the phase-locked device performance of MSTOGI-PLL with LADRC used in two different UPQC control systems during the grid voltage interruptions that happened in the three-phase three-wire power system, as illustrated in Figure 10. This refers to Figure 1, where the system shown is connected to a nonlinear load, and the UPQC output control accuracy and response speed are compared in both hysteresis control and FCS-MPC control systems. In one group, the phase-locked device adopts the MSTOGI-PLL improved based on LADRC, and the output quantities $v_{sa,h}$, $v_{sb,h}$, and $v_{sc,h}$ adopt a hysteresis control system. In the other group, the phase-locked device adopts the MSTOGI-PLL improved based on LADRC, and the output quantities $v_{sa,h}$, $v_{sb,h}$, and $v_{sc,h}$ adopt the FCS-MPC control system for improvement. By comparing the results between Figures 13(a) and 14(a), it can be seen that by-grid voltage interruptions have a great impact on the load voltage, v_{labc}, under hysteresis control utilized in the UPQC throughout 0–1 s. On the other hand, the grid voltage interruptions attributed to voltage swell and harmonic disturbances that occur between 0.1 and 0.4 s cause a noticeable distortion of the v_{labc} waveform due to ineffective compensation from UPQC using hysteresis control. This refers to a comparison between Figures 13(b) and 14(b). In Figure 14(b), the UPQC with FCS-MPC compensates with a uniform sinusoidal waveform of v_{labc} throughout 0.1–0.2 s, compared to the UPQC with hysteresis control illustrated in Figure 13(b). By referring to Figure 14(b), the slightly distorted waveform of v_{labc} after 0.3 s shows the robustness of the FCS-MPC in improving the UPQC performance as compared to the hysteresis control. The

distortion of the v_{labc} waveform gets worse within 0.2–0.4 s, subject to the compensation conducted by the UPQC using hysteresis control, as illustrated in Figure 13(b).

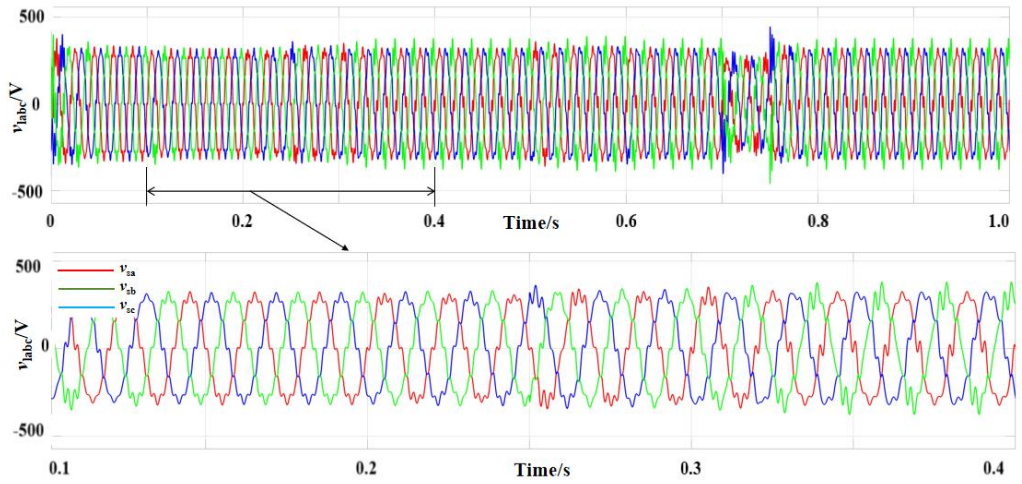


Figure 13. Load voltage, v_{labc}, waveform under hysteresis control of UPQC (a) within the period of 0–1 s, and (b) enlarged view of the period 0.1–0.4 s.

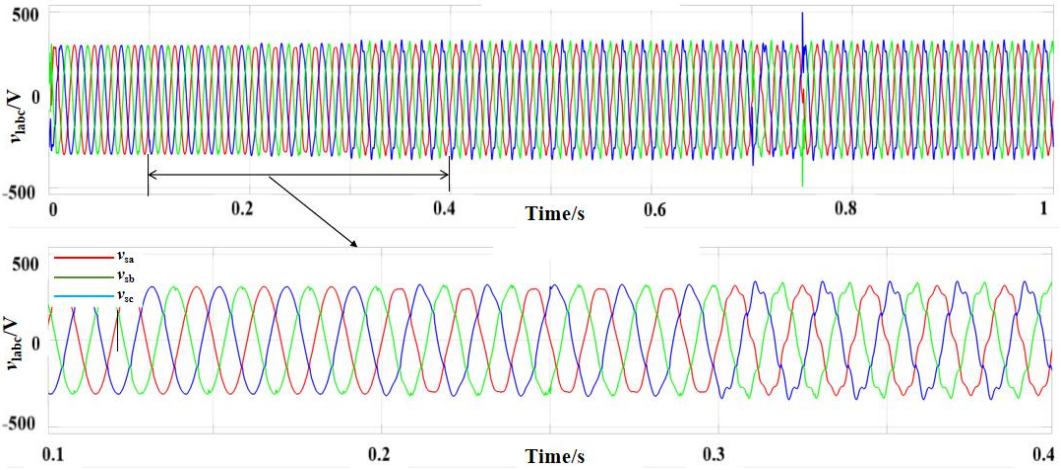


Figure 14. Load voltage, v_{labc}, waveform under FCS-MPC of UPQC (a) within the period of 0–1 s, and (b) enlarged view of the period 0.1–0.4 s.

The comparison of Figures 15(a) and 16(a) shows that the hysteresis control of UPQC fails to compensate for the grid voltage interruptions given in Figure 10, leading to load current, i_{labc}, waveform sagging between 0.7 and 0.75 s. However, contrary to the FCS-MPC utilized in UPQC, there is no i_{labc} waveform sagging between 0.7 and 0.75 s. Figures 15(b) and 16(b) reveal that the nonlinear load with a temporary rise in harmonic disturbance causes slight distortion of the two identical i_{labc} waveforms after the compensation performed by hysteresis control and FCS-MPC of UPQC, respectively.

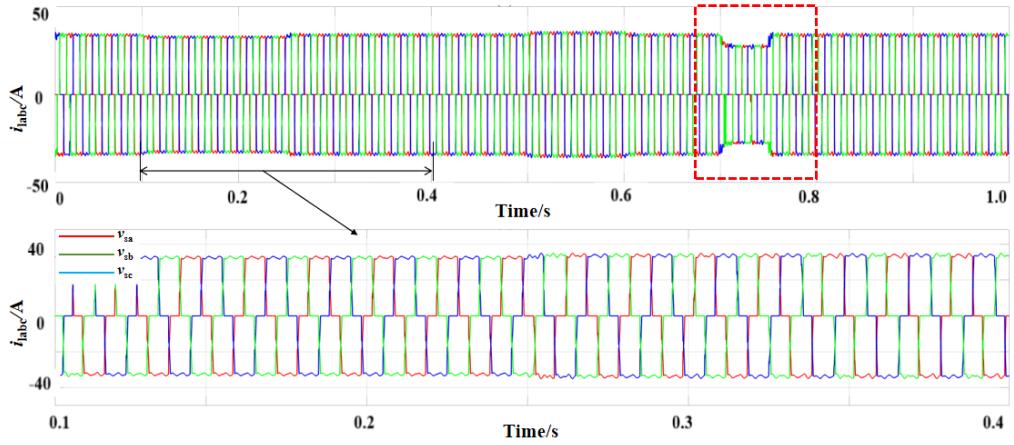


Figure 15. Load current, i_{labc}, waveform under hysteresis control of UPQC, (a) within the period of 0–1 s, and (b) enlarged view of the period 0–0.4 s.

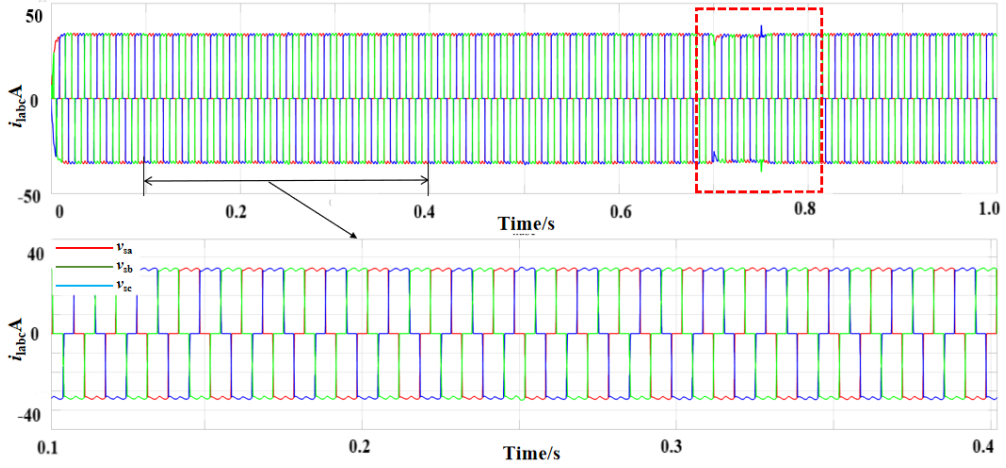


Figure 16. Load current, i_{labc}, waveform under FCS-MPC of UPQC, (a) within the period of 0–1 s, and (b) enlarged view of the period 0–0.4 s.

Furthermore, in Figure 17 and Table 4, it is proven that the FCS-MPC in UPQC significantly reduces the THD value of load voltage, v_l, during grid voltage sags and swells, as compared to the hysteresis control in UPQC.

Table 4. THD value of v_l under different control systems in UPQC.

Disturbance type	THD of load voltage subject to FCS-MPC in UPQC	THD of load voltage subject to hysteresis control in UPQC
Voltage sag	1.1%	9.03%
Voltage swell	7.82%	13.87%

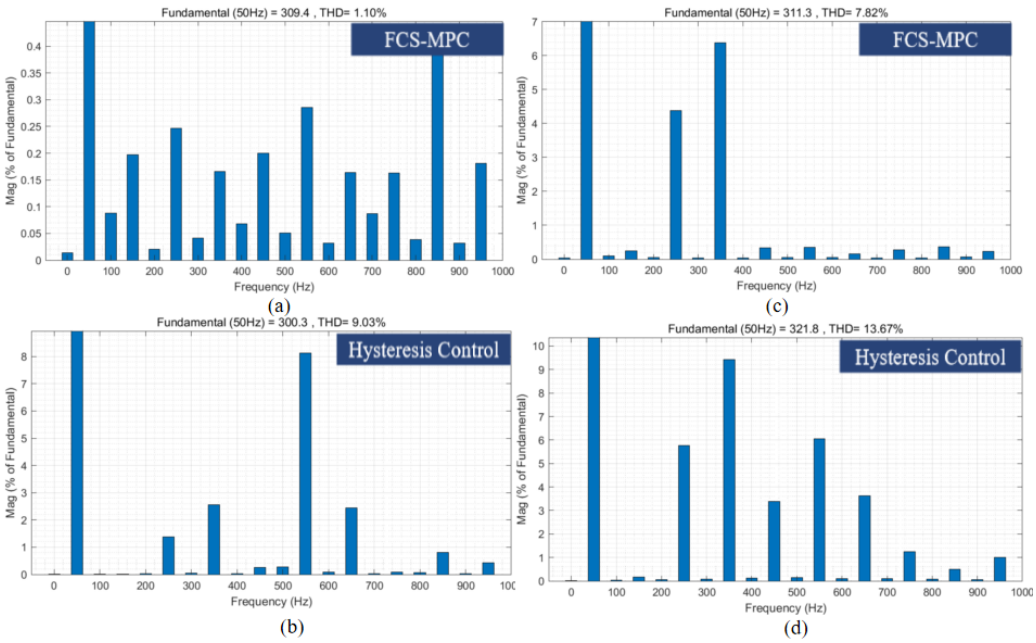


Figure 17. THD value of load voltage, v_l, for (a) FCS-MPC in UPQC during v_s sag, (b) hysteresis control in UPQC during v_s sag, (c) FCS-MPC in UPQC during v_s swell, and (d) hysteresis control in UPQC during v_s swell.

In case IV, the MSTOGI-PLL with LADRC is used in UPQC for compensation in the three-phase three-wire power system connected to a linear load shown in Figure 1 that considers the impact of grid voltage disturbances as given in Figure 10. The MSTOGI-PLL with LADRC in UPQC is performed based on the two conditions of hysteresis control and FCS-MPC. The importance of hysteresis control and FCS-MPC to improve the performance of UPQC can be observed by referring to the compensation accuracy and response of load voltage and current waveforms that can be seen in Figures 19 and 20, respectively.

The comparison between the results illustrated in Figures 18(a) and 18(c) indicates that the FCS-MPC enhances the UPQC performance by maintaining a stable load voltage, v_{la}, waveform, contradicting the load voltage, v_{la}, waveform distortion at 0.7–0.75 s caused by an ineffective hysteresis control used in UPQC. The findings are supported by a thorough investigation of the v_{la} waveform, specifically focusing on the period of 0.6–0.85 s, as depicted in Figures 18(b) and 18(d). Figure 18(d) shows that the hysteresis control does not improve the UPQC performance in compensation, resulting in an adverse v_{la} waveform distortion at 0.7–0.76 s, as opposed to the minor v_{la} waveform distortion merely at 0.75 s, caused by a significant impact of FCS-MPC that improves the UPQC compensation performance, as depicted in Figure 18(a).

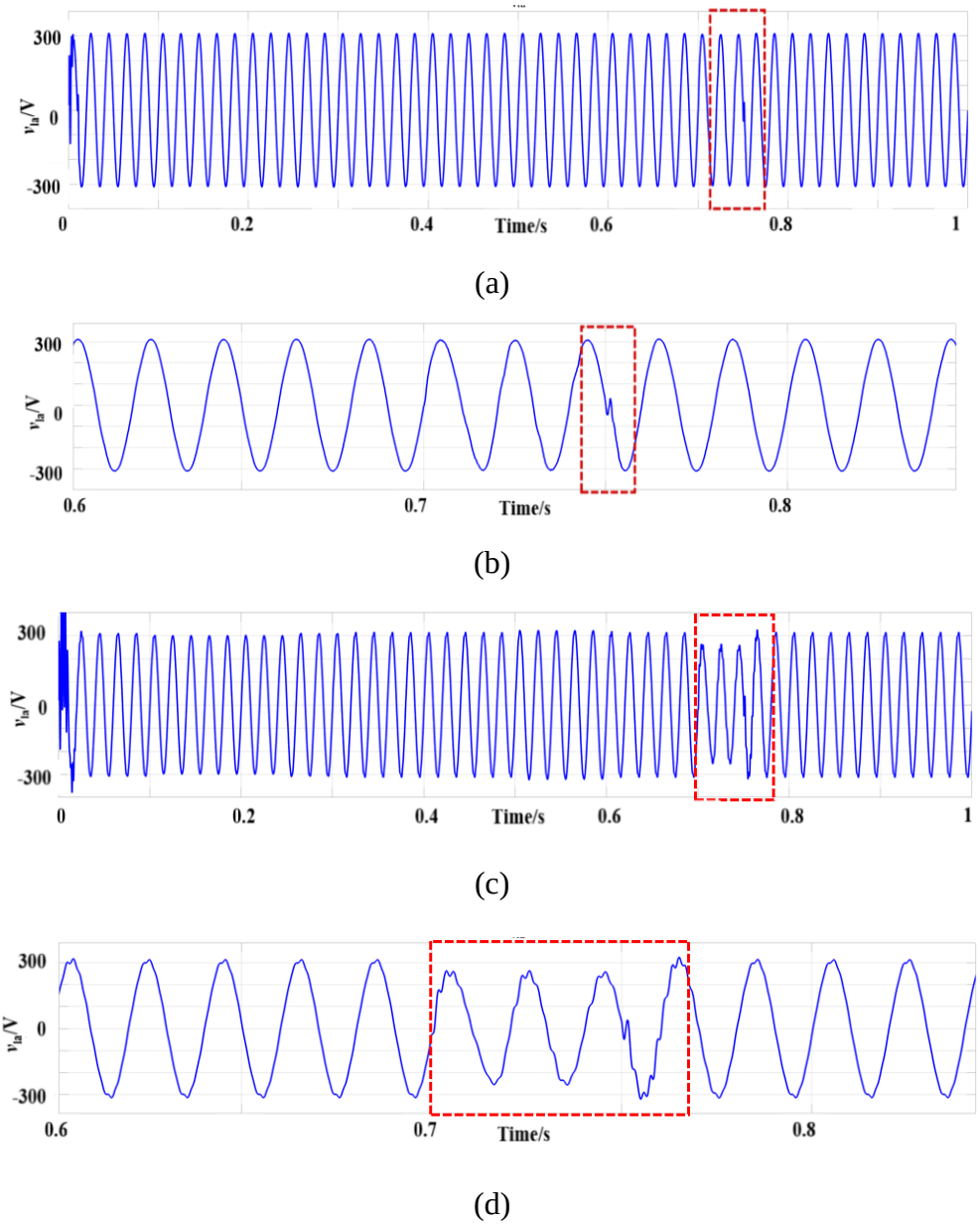


Figure 18. Load voltage, v_{la} , waveforms (a) at 0–1s acquired from UPQC with FCS-MPC, (b) at 0.6–0.85 s acquired from UPQC with FCS-MPC, (c) at 0–1 s acquired from UPQC with hysteresis control, and (d) at 0.6–0.85 s acquired from UPQC with hysteresis control.

The comparative result in Figures 19(a) and 19(c) signifies that the FCS-MPC in UPQC can compensate for the disturbances, yielding a constantly stable load current, i_{la}, waveform; albeit there are grid voltage interruptions within 0.7–0.75 s. Nevertheless, it is different from the deficient UPQC performance considering hysteresis control in which acute i_{la} waveform distortion is evident during the period of 0.7–0.75 s. In addition, there is a slight distortion of the i_{la} waveform at 0.75 s attained from the UPQC under the two control systems, as presented in Figures 19(b) and 19(d).

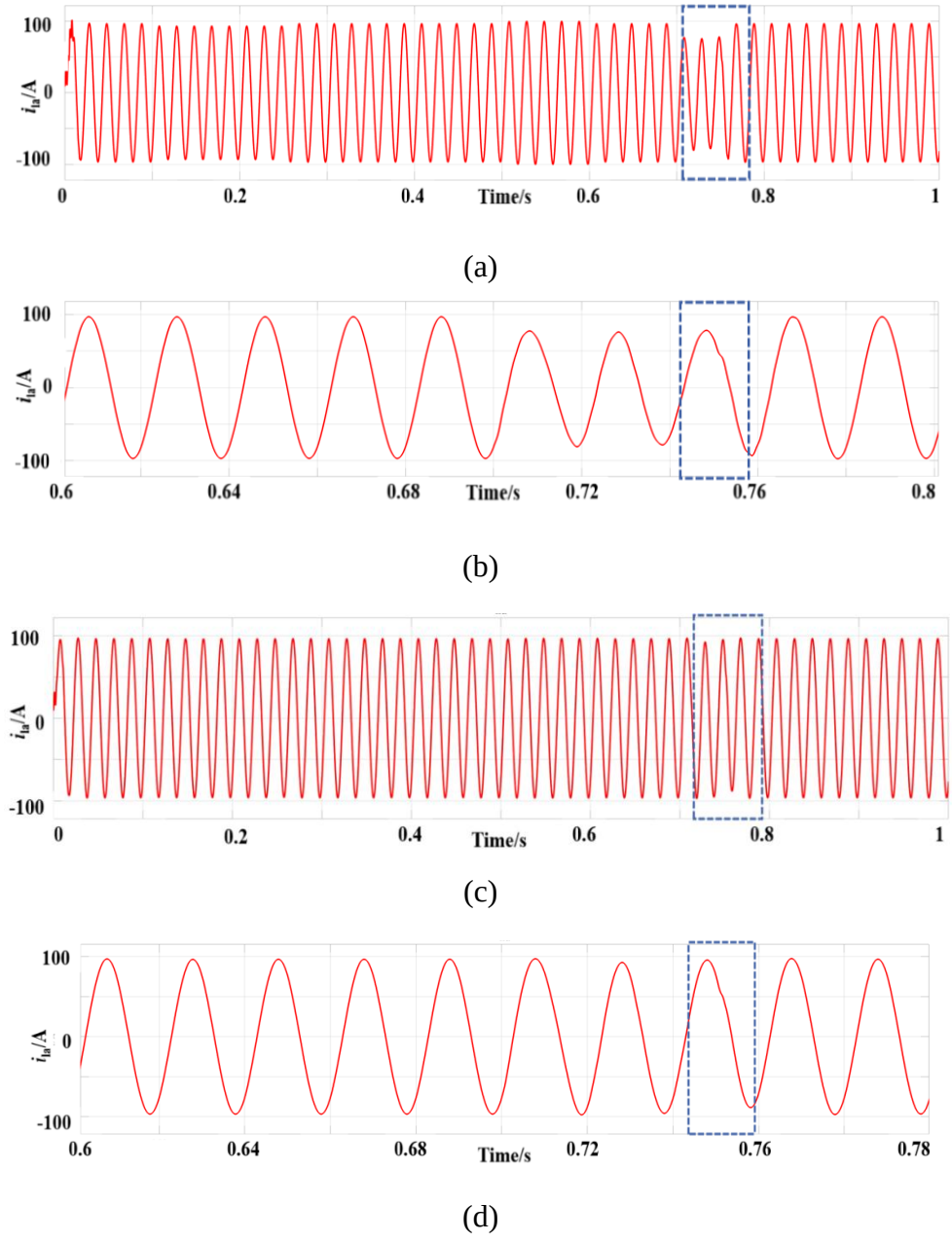


Figure 19. Load current, i_{la}, waveforms (a) at 0–1 s under UPQC with FCS-MPC, (b) at 0.6–0.8 s under UPQC with FCS-MPC, (c) at 0–1 s under UPQC with hysteresis control, and (d) at 0.6–0.8 s under UPQC with hysteresis control.

6. Conclusions

This research presents an enhanced UPQC compensation system for a low-voltage 380 V three-phase three-wire power system. The enhancement primarily comprises two components: 1) deploying an MSTOOGI-PLL supported by LADRC, and 2) employing a control system based on FCS-MPC. Owing to enhancements in the phase-locked loop controller, simulation tests evaluated the MSTOOGI-PLL+PI, MSTOOGI-PLL+LADRC, and traditional SRF-PLL+PI phase-locked loop systems under diverse disturbance situations. The hysteresis control and FCS-MPC control systems

were compared for the enhancement of the control system. Simulation analysis indicates that the proposed LADRC-enhanced FCS-MPC system significantly improves harmonic suppression (diminishing load-side voltage THD), dynamic disturbance mitigation, and post-compensation power quality during grid anomalies (encompassing voltage fluctuations, harmonic distortion, and transient interruptions). The principal findings of the investigation are summarized as follows:

(1) The LADRC-optimized MSTOGI-PLL exhibits accelerated response characteristics with minimized overshoot and enhanced phase-tracking accuracy.
(2) Simulation result comparisons of three-phase-locking configurations reveal that the LADRC-enhanced MSTOGI-PLL reduces load-side voltage fluctuations by 41.7% during grid disturbances, thereby improving the UPQC compensation efficacy by 28.9%.
(3) Assuming that the MSTOGI phase-locking device utilizes LADRC as the controller when subjected to a nonlinear load, the output voltage on the load side of the UPQC system governed by FCS-MPC control demonstrates enhanced disturbance resistance and a reduced THD value for the load side output.
(4) For linear load scenarios, the proposed system maintains superior anti-disturbance performance with 1.1% voltage THD during sag conditions and 7.82% THD during swell events, outperforming conventional hysteresis control by 87.8% and 43.6%, respectively.

Author contributions

Yuting Yu and Yanting Chu: Conceptualization, simulation, writing – original draft; Muhammad Murtadha Othman and Ismail Musirin: Analysis, drafting and editing of the manuscript.

Use of Generative-AI tools declaration

The authors declare they have not used Artificial Intelligence (AI) tools in the creation of this article.

Acknowledgments

This research was funded by Hunan Provincial Department of Education Scientific Research Project (Outstanding Youth Project), grant number “23B1016”.

This research was also supported by the Strategic Research Partnership (SRP) with project code 100-RMC 5/3/SRP INT (012/2024) under the Research Management Centre (RMC), Universiti Teknologi MARA (UiTM), Shah Alam, Selangor, Malaysia.

Conflict of interest

On behalf of all authors, the corresponding author declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

References

1. Qasim AY, Tahir FR, Alsammak ANB (2024) Improving Power Quality in Distribution Systems Using UPQC: An Overview. *Journal Européen des Systèmes Automatisés* 57.

https://doi.org/10.18280/jesa.570201
2. Jin T, Chen Y, Guo J, Wang M, Mohamed MA (2020) An effective compensation control strategy for power quality enhancement of unified power quality conditioner. *Energy Reports* 6: 2167–2179. https://doi.org/10.1016/j.egyr.2020.07.027
3. Farooq A, Bhat AH (2024) Simplified control strategy-based three-phase reduced switch UPQC for mitigation of power quality problems. *International Journal of Power Electronics* 20: 266–300. https://doi.org/10.1504/IJPELEC.2024.142280
4. Palanisamy T, Thangamuthu GS (2024) Optimal power quality improvement in distribution system with UPQC using an improved strategy. *Optimal Control Applications and Methods* 45: 1433–1455. https://doi.org/10.1002/oca.3105
5. Feng D, Chen T, Zhang L, Meng W, He J (2024) A control method for the single-phase three-leg unified power quality conditioner without a phase-locked loop. *Front Energy Res* 12: 1343520. https://doi.org/10.3389/fenrg.2024.1343520
6. Han J, Li X, Jiang Y, Gong S (2021) Three-Phase UPQC Topology Based on Quadruple-Active-Bridge. *IEEE Access* 9: 4049–4058.
7. Yadav SK, Yadav KB, Priyadarshi A (2024) Performance analysis of three-phase solar PV, BESS, and Wind integrated UPQC for power quality improvement. *Computers and Electrical Engineering* 116: 109230. https://doi.org/10.1016/j.compeleceng.2024.109230
8. Kanchana K, Babu V, Gaddam S, Naidu Pudi V (2025) Advancing microgrid power quality: integration of GRU-based control in PV-UPQC systems. *Electr Eng* 107: 223–248. https://doi.org/10.1007/s00202-024-02517-2
9. Nicola M, Nicola CI, Sacerdoțianu D, Vintilă A (2023) Comparative performance of UPQC control system based on PI-GWO, fractional order controllers, and reinforcement learning agent. *Electronics* 12: 494. https://doi.org/10.3390/electronics12030494
10. Fuyin NI, Jian H (2023) Research on UPQC harmonic control strategy based on optimized QPIR controller of beetle antennae search algorithm in microgrid. *Electr Eng* 106: 2357–2369. https://doi.org/10.1007/s00202-023-02066-0
11. Yadav SK, Yadav KB (2023) FOPI Controller with Chicken Swarm Optimization for Power Quality Improvement of HES System Integrated UPQC. *Computational Vision and Bio-Inspired Computing: Proceedings of ICCVBIC 2022*, 367-378. Singapore: Springer Nature Singapore. https://doi.org/10.1007/978-981-19-9819-5_28
12. Kumar GS, Kumar BK, Mishra MK (2011) Mitigation of Voltage Sags With Phase Jumps by UPQC With PSO-Based ANFIS. *IEEE T Power Deliver* 26: 2761–2773. https://doi.org/10.1109/TPWRD.2011.2165301
13. Zanib N, Batool M, Riaz S, Nawaz F (2022) Performance Analysis of Renewable Energy Based Distributed Generation System Using ANN Tuned UPQC. *IEEE Access* 10: 110034–110049. https://doi.org/10.1109/ACCESS.2022.3213948
14. Kumar A, Kumar P (2024) JAYA based optimization strategy for UPQC PI tuning based on novel SRF-DSOGI PLL control. *Int J Syst Assur Eng Manag* 15: 3193–3209. https://doi.org/10.1007/s13198-024-02325-8
15. Bueno-Contreras H, Ramos GA, Costa-Castelló R (2021) Power quality improvement through a upqc and a resonant observer-based mimo control strategy. *Energies* 14: 6938. https://doi.org/10.3390/en14216938
16. Xu J, Qian H, Qian Q, Xie S (2023) Modeling, Stability, and Design of the Single-Phase

SOGI-Based Phase-Locked Loop Considering the Frequency Feedback Loop Effect. *IEEE T Power Electr* 38: 987–1002. https://doi.org/10.1109/TPEL.2022.3201252
17. Hui N, Feng Y, Han X (2020) Design of a High Performance Phase-Locked Loop With DC Offset Rejection Capability Under Adverse Grid Condition. *IEEE Access* 8: 6827–6838. https://doi.org/10.1109/ACCESS.2020.2963993
18. Li G, Chen Y, Luo A, Wang Y (2021) An Inertia Phase Locked Loop for Suppressing Sub-Synchronous Resonance of Renewable Energy Generation System Under Weak Grid. *IEEE T Power Syst* 36: 4621–4631. https://doi.org/10.1109/TPWRS.2021.3066481
19. Alam SJ, Arya SR (2020) Control of UPQC based on steady state linear Kalman filter for compensation of power quality problems. *Chinese Journal of Electrical Engineering* 6: 52–65. https://doi.org/10.23919/CJEE.2020.000011

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