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Research article

Adaptive fixed-frequency hysteresis band control method for UPQC

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Abstract: This paper proposes an adaptive fixed-frequency hysteresis band control method for a unified power quality conditioner (UPQC). First, a detailed analysis of the mathematical model and control for UPQC is performed. The series inverter is controlled to compensate for harmonic distortions in the source voltage, thereby maintaining a balanced voltage waveform applied to the load with harmonic distortion within permissible limits. Simultaneously, the shunt inverter is controlled to compensate for the current harmonics generated by nonlinear loads. The reference voltage for compensation is determined based on the distorted source voltage, while the reference harmonic current is derived using the i_p–i_q harmonic detection method. The harmonic mitigation performance of the UPQC is evaluated under two control scenarios. In Scenario 1, a conventional proportional integral (PI) controller is used for DC-link voltage regulation, and traditional hysteresis band controllers are used for both the series and shunt inverters. In Scenario 2, a fuzzy-PI controller is applied for DC-link voltage regulation, along with an adaptive fixed-frequency hysteresis band controller for both the series and shunt inverters. Simulation and experimental results under ideal, sag, swell, unbalanced, and distorted source-voltage conditions demonstrate that Scenario 2 is more effective than Scenario 1 in reducing the total harmonic distortion (THD) of the supply current and the load voltage and in stabilizing the DC-link voltage.

Keywords: unified power quality conditioner (UPQC); active power filter; hysteresis controller; PI controller; fuzzy controller; fuzzy-PI controller; DC-link voltage

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1. Introduction

Nowadays, power electronic converters are widely utilized in various fields due to their availability and flexibility. However, the widespread use of these converters introduces significant harmonic components into the power system, consequently deteriorating power quality. A simple approach to eliminate these harmonics is the use of passive power filters (PPFs) [1]. PPFs feature a simple structure and are easy to implement. Nevertheless, they suffer from several drawbacks, including sensitivity to environmental conditions, the potential for resonance with the system impedance, and unsuitability under varying load conditions. To overcome these limitations, active power filters (APFs) were developed. There are two main configurations of APFs: shunt APF [2] and series APF [3]. The shunt APF is effective at mitigating load current harmonics but cannot cancel source-side voltage harmonics. Conversely, the series APF can eliminate voltage harmonics from the source but is ineffective against current harmonics generated by nonlinear loads. In practical power systems, harmonic disturbances can originate from both the load and the source sides. Hence, the development of the UPQC has become essential [4–6]. The UPQC is an integrated system comprising a shunt APF and a series APF connected via a common DC link. It is a multifunctional device capable of compensating for a wide range of power quality issues, including voltage harmonics, imbalances, flicker, sags, and swells, as well as current-related disturbances such as harmonics, imbalances, and reactive currents.

Most studies on UPQC focus on improving the structure and control of the shunt inverter and series inverter and on stabilizing the DC-link voltage. UPQC structures come in many different forms [7–9], mainly differing in the structure of the shunt inverter and series inverter. The common objective of all these structures is to reduce the number of semiconductor components, reduce switching losses, and improve the dynamic response of the inverter to achieve better compensation performance for the UPQC. The controllers used to control UPQC's shunt inverters and inverter series include PI controllers [10–13], fuzzy logic [14,15], neural networks [16–18], PI-neural [19], and hybrid fuzzy-neural controllers [20,21]. The PI controller is less flexible in control situations where system parameters change. The fuzzy logic controller is flexible, easy to define, and does not require a detailed mathematical model, but the results are only moderately acceptable. Neural network controllers are suitable for online control and predictive control based on system changes, but their response is slow, and their structure is complex. Therefore, to achieve high control efficiency, these controllers are often combined to form hybrid controllers, such as fuzzy-PI, PI-neural, and fuzzy-neural. Previous works [22,23] used passivity fractional-order sliding mode control to improve the efficiency and sustainability of UPQC. A very effective control method also used for UPQC is active disturbance rejection control (ADRC) [24]. ADRC techniques are integrated to manage power flow, suppress active errors, and enhance the system's noise immunity; however, it is too complex. The DC-link voltage is typically regulated by comparing the reference value and the actual measured value at the DC-link, sent through a PI controller [10] to create a loss current that needs to be compensated to keep the DC-link voltage stable. This loss current will be fed into the instantaneous active current component to create the reference compensation current. Because the DC-link voltage varies during operation, a fuzzy regulator is used to tune the PI controller and maintain a constant DC-link voltage.

In summary, all control methods using the above controllers are typically combined with pulse-width modulation (PWM), such as sinusoidal pulse-width modulation (SPWM) [25] and space vector modulation [26], and require precise control parameters and complete system information. Meanwhile, classical hysteresis band control [27] offers advantages such as simplicity, fast response, and ease of implementation. While it does not require any information about system parameters, it has drawbacks, such as an uncontrolled switching frequency and high steady-state error, resulting in increased switching losses and large ripple content in the source voltage or supply current. To improve the shortcomings of classical hysteresis band modulation and enhance the overall compensation effectiveness of the UPQC, this paper implements improvements in several parts of the UPQC system: DC-link voltage regulation is carried out using a fuzzy-PI controller, and compensation control of the shunt/series inverters is implemented using an adaptive fixed-frequency hysteresis band control method. This method is implemented to maintain a constant switching frequency regardless of changes in other system parameters. Thus, the control method presented in this paper has the advantages of fast response and a constant switching frequency. This is beneficial for designing output filter circuits for shunt inverters and series inverters, reducing electromagnetic interference and switching losses. To demonstrate the effectiveness of the proposed method, simulation and experimental results under various scenarios, including ideal, sag, swell, unbalance, harmonic distortion voltage conditions, and load changes, are presented and discussed in detail.

2. Structure and control of UPQC

The structure of a UPQC is shown in Figure 1. It consists of two main components: the shunt part, which is responsible for compensating the harmonic currents generated by nonlinear loads, and the series part, which compensates for the voltage harmonics generated from the source through a transformer connected in series with the system. These two components are interconnected via a common DC-link.

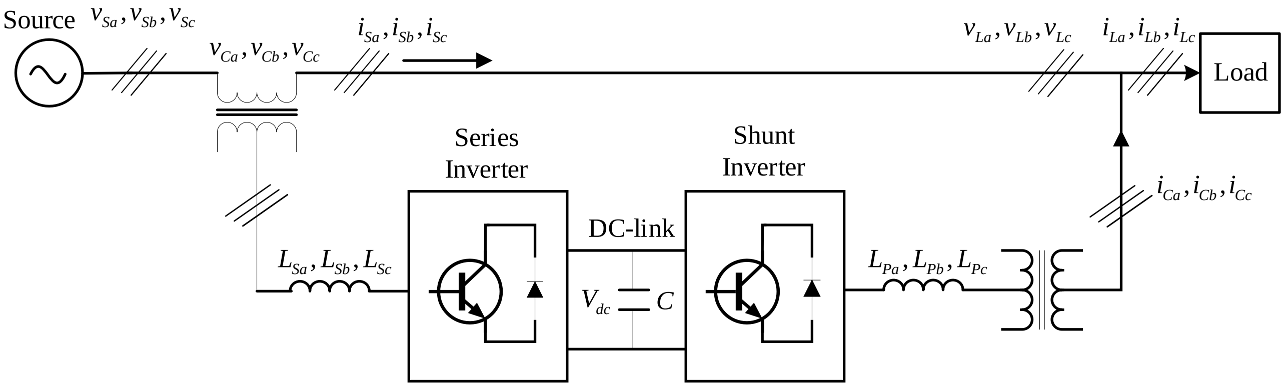


Figure 1. Structure of the unified power quality conditioner.

Where v_{Sa}, v_{Sb}, v_{Sc} are the three-phase source voltages; i_{Sa}, i_{Sb}, i_{Sc} are the three-phase supply currents; v_{La}, v_{Lb}, v_{Lc} are the three-phase load voltages; i_{La}, i_{Lb}, i_{Lc} are the three-phase load currents; i_{Ca}, i_{Cb}, i_{Cc} are the three-phase compensating currents from the shunt inverter; v_{Ca}, v_{Cb}, v_{Cc} are the three-phase compensating voltages from the series inverter; L_{Sa}, L_{Sb}, L_{Sc} are the three-phase output filters of the series inverter; and L_{Pa}, L_{Pb}, L_{Pc} are the three-phase output filters of the shunt inverter. The series and shunt inverters operate based on reference harmonic voltages and currents, which are determined from the source voltages and load currents. The method for determining the reference harmonic voltages and controlling the series inverter is illustrated in Figure 2. The three-phase source voltages are sent through a phase-locked loop (PLL) to generate an output ωt, which also implies keeping the input and output frequencies the same. Then, two additional signals shifted by $120\,°$ are generated to form a set of three unit-amplitude waveforms. These waveforms are then multiplied by the source voltage magnitude V_m to produce the fundamental components of the reference three-phase voltages $v_{La}^*, v_{Lb}^*, v_{Lc}^*$. The fundamental three-phase voltages to be applied to the load are defined as follows:

$$\begin{bmatrix} v_{La}^* \\ v_{Lb}^* \\ v_{Lc}^* \end{bmatrix} = [V_m] \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - 2\pi/3) \\ \sin(\omega t + 2\pi/3) \end{bmatrix} \tag{1}$$

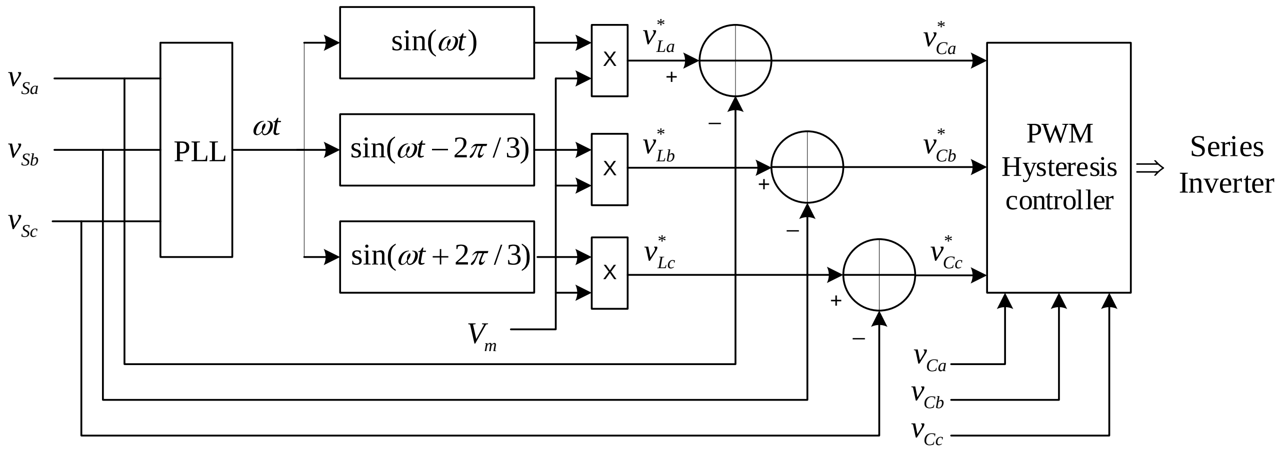


Figure 2. Method for determining reference harmonic voltage and controlling the series inverter.

The reference harmonic voltage components are determined as follows:

$$\begin{aligned} v_{Ca}^* &= v_{La}^* - v_{Sa} \\ v_{Cb}^* &= v_{Lb}^* - v_{Sb} \\ v_{Cc}^* &= v_{Lc}^* - v_{Sc} \end{aligned} \tag{2}$$

These reference harmonic voltage components are then compared with the actual voltages v_{Ca}, v_{Cb}, v_{Cc}, and the resulting error signals are used to generate the gating pulses for the series inverter.

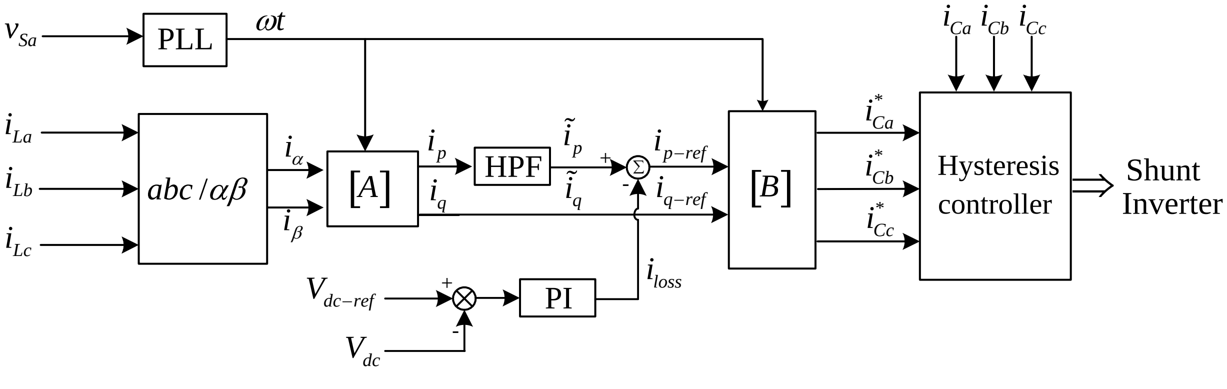


Figure 3. Method for determining the reference harmonic current and controlling the shunt inverter.

The method for determining the reference harmonic currents [19] is illustrated in Figure 3. i_α and i_β are obtained from the transformation of the *abc* coordinate system to the *αβ* coordinate system.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{3}$$

The instantaneous active and reactive current components are:

$$\begin{bmatrix} i_p \\ i_q \end{bmatrix} = [A] \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{4}$$

Where $[A] = \begin{bmatrix} \sin\omega t & -\cos\omega t \\ \cos\omega t & \sin\omega t \end{bmatrix}$

Using a high-pass filter (HPF) to extract the AC components of i_p is $\tilde{i}_p$.

To compensate for harmonic current components from the load and stabilize the DC-link voltage, the reference values for i_p and i_q will be:

$$\begin{bmatrix} i_{p-ref} \\ i_{q-ref} \end{bmatrix} = \begin{bmatrix} \tilde{i}_p - i_{loss} \\ i_q \end{bmatrix} \tag{5}$$

Accordingly, the reference compensating currents are determined as follows:

$$\begin{bmatrix} i_{Ca}^* \\ i_{Cb}^* \\ i_{Cc}^* \end{bmatrix} = [B] \begin{bmatrix} i_{p-ref} \\ i_{q-ref} \end{bmatrix} \tag{6}$$

Where $[B] = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \sin\omega t & \cos\omega t \\ -\cos\omega t & \sin\omega t \end{bmatrix}$

3. Adaptive fixed-frequency hysteresis band control for UPQC

3.1. Design of fuzzy-PI controller for DC-link voltage stabilization of UPQC

DC-link voltage stabilization is one of the most critical tasks that determines the compensation effectiveness and stability of a UPQC system. The cause of voltage fluctuations in the DC-link is due to changing load or power source and losses in parasitic resistors in semiconductor valves, inductors, and capacitors. Since V_{dc-ref} is a constant, a conventional PI controller is commonly used in this control loop [11,12]. However, the DC-link voltage continuously varies, whereas the PI controller gains remain fixed during operation. Therefore, a conventional PI controller may not be suitable when the DC-link voltage changes dynamically. To address this issue, this paper designs a fuzzy-PI controller to regulate the DC-link voltage of the UPQC. The error between the reference voltage V_{dc-ref} and the actual voltage V_{dc} is passed through a fuzzy-PI controller and then added to the instantaneous active power component in the i_p-i_q harmonic current detection block. The DC-link voltage regulation scheme is presented in Figure 4.

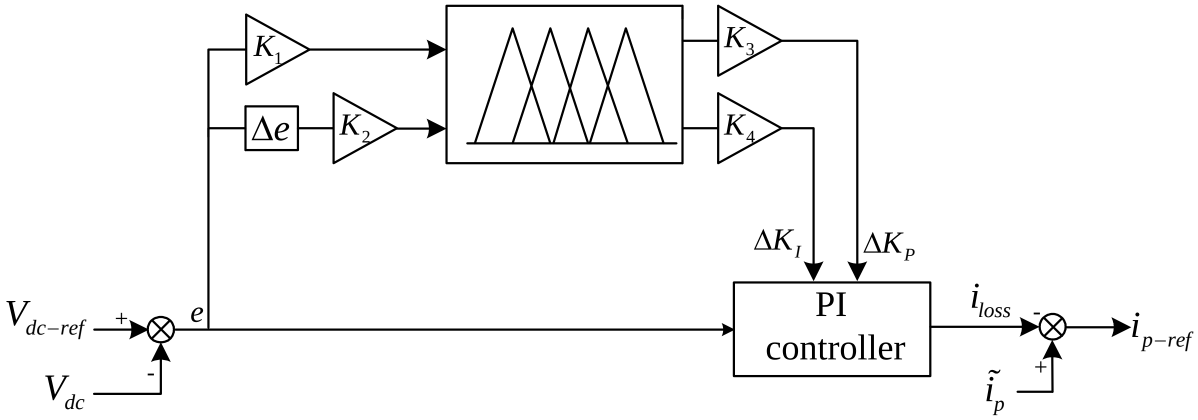


Figure 4. Fuzzy-PI controller for DC-link voltage stabilization.

The inputs of the fuzzy controller are the error (e) and the change of the error (Δe). The outputs of the fuzzy controller are ΔK_P and ΔK_I. K_1, K_2, K_3, and K_4 are the tuning coefficients for inputs and outputs compatibility. Then, the adjusted K_P and K_I values will be:

$$\begin{aligned} K_{P-new} &= K_{P-old} + \Delta K_P \\ K_{I-new} &= K_{I-old} + \Delta K_I \end{aligned} \tag{7}$$

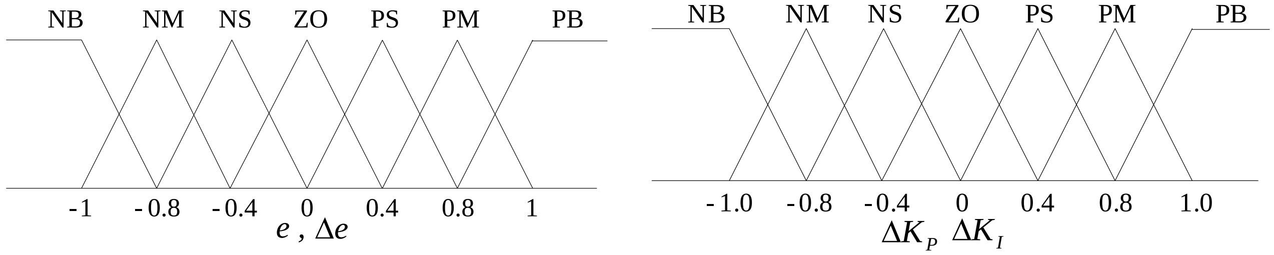
To implement fuzzy control, the inputs and outputs are fuzzified into linguistic variables, including negative big (NB), negative medium (NM), negative small (NS), zero (ZO), positive small (PS), positive medium (PM), and positive big (PB), as shown in Figure 5. Figure 5(a) shows the membership functions of the input variables, and Figure 5(b) shows the membership functions of the output variables.

The core of the fuzzy controller lies in the fuzzy control rules; the principle for adjusting ΔK_P and ΔK_I is as follows:

- Adjustment principle ΔK_P: When the error e is large (V_{dc} deviates significantly from V_{dc-ref}), then a sufficiently large value of K_P is needed. This means that ΔK_P must be PB or PM so that the system responds quickly and provides immediate compensation current. When the error e is small (V_{dc}

approaches V_{dc-ref}), K_P needs to be reduced, meaning ΔK_P must be PS or ZO to avoid overvoltage across the capacitor.

- Adjustment principle ΔK_I: When the error *e* is large (V_{dc} deviates significantly from V_{dc-ref}), then K_I must be kept small or equal to zero. Therefore, ΔK_I must be NB or NM to avoid saturation, which causes strong oscillations. When the error *e* is small and *de* is small (the system is about to reach steady state), it is necessary to increase K_I (i.e., ΔK_I must be PB or PM) to completely eliminate the steady-state error and make V_{dc} closely follow V_{dc-ref}. Based on the above rules, the fuzzy control rules of ΔK_P and ΔK_I are summarized in Table 1.

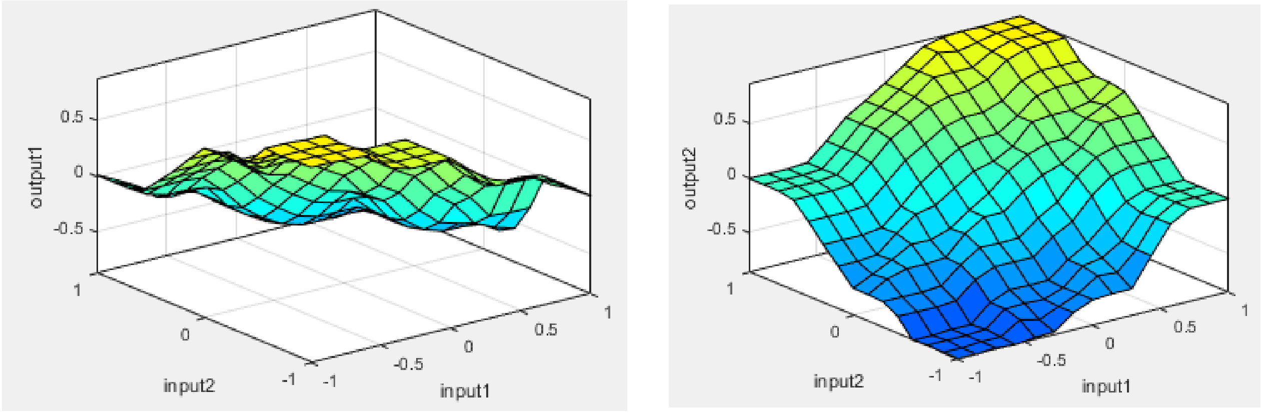


(a) (b)

Figure 5. Membership functions of the input and output variables of the fuzzy controller; (a) membership functions of input variables; (b) membership functions of output variables.

Table 1. Fuzzy control rules of ΔK_P and ΔK_I.

$\Delta K_P / \Delta K_I$		*de*						
		NB	**NM**	**NS**	**ZO**	**PS**	**PM**	**PB**
e	**NB**	PB/NB	PB/NB	PM/NM	PM/NM	PS/NS	Z0/ZO	Z0/ZO
	NM	PB/NB	PB/NB	PM/NM	PS/NS	PS/NS	Z0/ZO	Z0/ZO
	NS	PM/NB	PM/NM	PM/NS	PS/NS	Z0/ZO	NS/PS	NS/PS
	ZO	PM/NM	PM/NM	PS/NS	Z0/ZO	NS/PS	NM/PM	NM/PM
	PS	PS/NM	PS/NS	Z0/ZO	NS/PS	NS/PS	NM/PM	NM/PB
	PM	PS/ZO	Z0/ZO	NS/PS	NM/PS	NM/PM	NM/PB	NB/PB
	PB	Z0/ZO	Z0/ZO	NM/PS	NM/PM	NM/PM	NB/PB	NB/PB



(a) (b)

Figure 6. Control surface of the fuzzy controller in Figure 4; (a) surface of the inputs and output1; (b) surface of the inputs and output2.

The defuzzification process uses the centroid method. The surface of fuzzy control is shown in Figure 6. The surface of the fuzzy controller demonstrates that fuzzy control laws do not produce abrupt changes, have no extremes, and gradually decrease to zero.

3.2. Design of an adaptive fixed-frequency hysteresis band control method for the shunt inverter

The inverter considered here is a three-phase two-level voltage source inverter, where leg "*a*" consists of S_1 upper and S_4 lower, leg "*b*" consists of S_3 upper and S_6 lower, and leg "*c*" consists of S_5 upper and S_2 lower. Consider the hysteresis current controller in one switching cycle, as illustrated in Figure 7, based on [28]. Focusing on a single phase (leg "*a*"), the general expression representing the current increase during the time when switch S_1 is ON can be written as:

$$\Delta HB_{ia} = \frac{t_{1n}}{L_{Pa}}(V_{dc} - v_{La}) - t_{1n}\frac{di_{Ca}^*}{dt} \tag{8}$$

Therefore, the hysteresis band width during the current rising interval is:

$$2HB_{ia} = \sum \Delta HB_{ia} = -t_1\left(\frac{di_{Ca}^*}{dt} + \frac{v_{La}}{L_{Pa}}\right) + \frac{t_1}{L_{Pa}}V_{dc} \tag{9}$$

The general expression representing the current decrease during the time when S_4 ON is:

$$-\Delta HB_{ia} = \frac{t_{2n}}{L_{Pa}}(V_{dc} + v_{La}) - t_{2n}\frac{di_{Ca}^*}{dt} \tag{10}$$

Therefore, the hysteresis band width during the current falling interval is:

$$-2HB_{ia} = \sum -\Delta HB_{ia} = -t_2\left(\frac{di_{Ca}^*}{dt} + \frac{v_{La}}{L_{Pa}}\right) - \frac{t_2}{L_{Pa}}V_{dc} \tag{11}$$

Where $t_1 + t_2 = T_c = \frac{1}{f_{sw}}; t_1 = \sum t_{1n}; t_2 = \sum t_{2n}$; t_1 and t_2 are the respective switching intervals, and f_{sw} is the switching frequency.

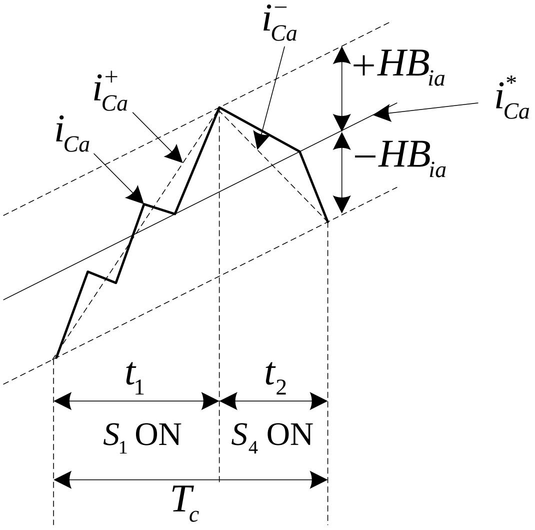


Figure 7. Hysteresis current controller in one switching cycle.

From (9) and (11), the adaptive hysteresis band can be derived as follows:

$$HB_{ia} = \frac{V_{dc}}{4f_{sw}L_{Pa}}\left[1 - \frac{L_{Pa}^2}{V_{dc}^2}\left(\frac{di_{Ca}^*}{dt} + \frac{v_{La}}{L_{Pa}}\right)^2\right] \tag{12}$$

$$f_{sw} = \frac{V_{dc}}{4HB_{ia}L_{Pa}}\left[1 - \frac{L_{Pa}^2}{V_{dc}^2}\left(\frac{di_{Ca}^*}{dt} + \frac{v_{La}}{L_{Pa}}\right)^2\right] \tag{13}$$

Equations (12) and (13) indicate that HB_{ia} depends on the parameters f_{sw}, V_{dc}, L_{Pa}, i_{Ca}^*, and v_{La}. Assume V_{dc} is adjusted to a constant value as described in Section 3.1 and f_{sw}, L_{Pa} are fixed. Therefore, HB_{ia} is dependent on v_{La} and reference current i_{Ca}^*. However, in practice, the values of parameters V_{dc}, L_{Pa}, i_{Ca}^*, and v_{La} are variable, leading to a change in HB_{ia} and consequently a change in f_{sw}. Therefore, adjusting HB_{ia} according to formula (12) only makes the switching frequency less oscillating compared to using a traditional hysteresis control, but it cannot fix the switching frequency. To keep the inverter switching frequency constant, the paper uses a fuzzy controller to compensate for the HB_{ia} value when the frequency measured at the inverter (f_{act}) is different from the reference frequency (f_{ref}). The diagram using the fuzzy controller to keep the switching frequency constant is shown in Figure 8, where K_e, K_{e_f}, and K_{HB} are the tuning coefficients for inputs and outputs compatibility. Error e_f and variation of error Δe_f are the inputs, and ΔHB_{ia} is the output.

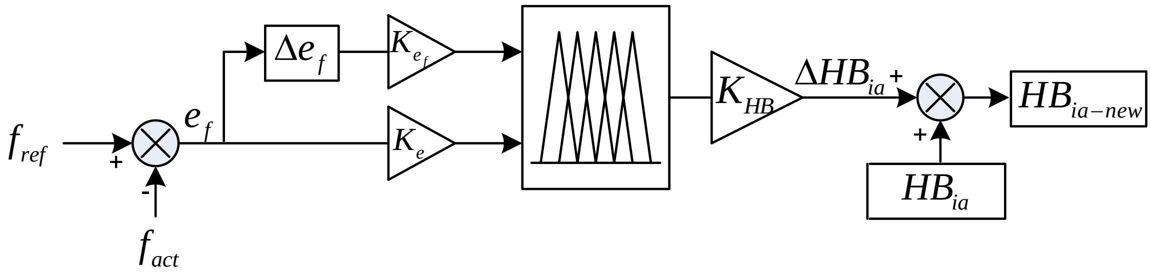
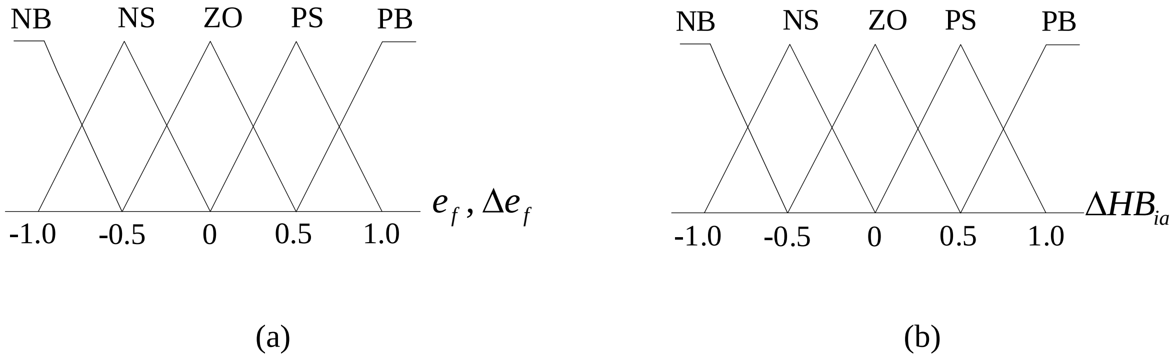


Figure 8. Design of a fuzzy controller for HB_{ia} adjustment.

The inputs and output of the fuzzy controller are fuzzified into linguistic values—negative big (NB), negative small (NS), zero (ZO), positive small (PS), and positive big (PB)—as shown in Figure 9. Figure 9(a) shows membership functions of the input variables, and Figure 9(b) shows membership functions of the output variable.



(a) (b)

Figure 9. Membership functions of the input and output variables of the fuzzy controller; (a) membership functions of input variables; (b) membership functions of the output variable.

Fuzzy control rules are built on the principle that since bandwidth HB_{ia} is inversely proportional to switching frequency, if e_f is PB (the actual frequency f_{act} is too low compared to the reference frequency f_{ref}), then HB_{ia} should be significantly reduced; if e_f is NB (the actual frequency f_{act} is too high compared to the reference frequency f_{ref}), then HB_{ia} should be significantly increased; and if e_f is ZO (the actual frequency f_{act} is equal to the reference frequency f_{ref}), then HB_{ia} should be kept constant. Based on the above principle, the fuzzy rule table is shown in Table 2. In this control scheme, the min–max method is employed for both fuzzification. The defuzzification process uses the centroid method. The adjusted HB_{ia} value is:

$$HB_{ia-new} = HB_{ia} + \Delta HB_{ia} \tag{14}$$

The surface of fuzzy control is shown in Figure 10.

Table 2. Fuzzy control rules.

ΔHB_{ia}		Δe_f				
		NB	**NS**	**ZO**	**PS**	**PB**
e_f	**NB**	PB	PB	PB	PS	ZO
	NS	PB	PS	PS	ZO	NS
	ZO	PS	PS	ZO	NS	NS
	PS	PS	ZO	NS	NS	NB
	PB	ZO	NS	NB	NB	NB

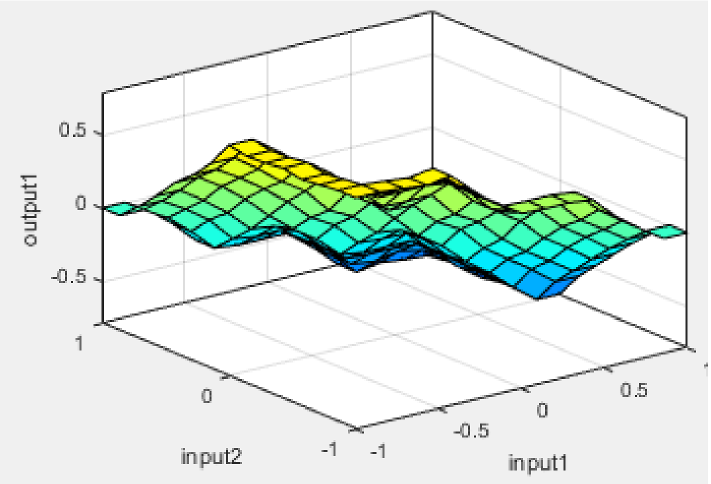


Figure 10. Control surface of the fuzzy controller.

$HB_{ia\text{-}new}$ is combined with the reference currents $i^*_{Ca}, i^*_{Cb}, i^*_{Cc}$ and actual currents i_{Ca}, i_{Cb}, i_{Cc} to generate gate pulses for the inverter switches, as illustrated in Figure 11.

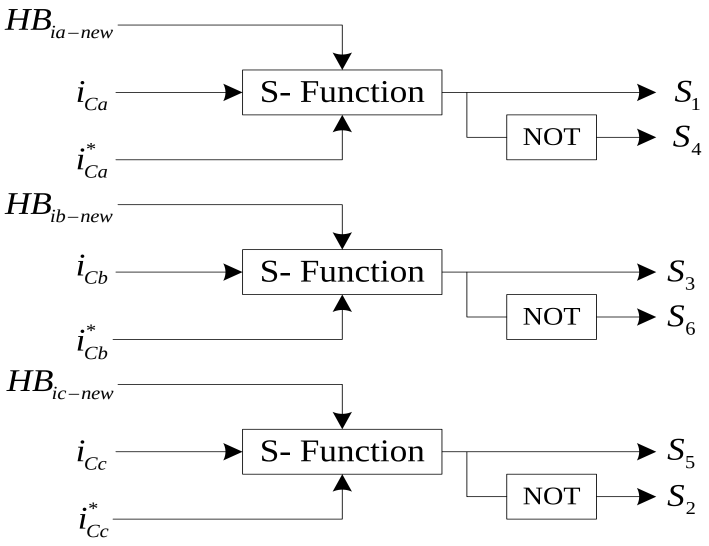


Figure 11. Pulse generation circuit for inverter switches.

The S-Function is written according to the rule: If $i_{Ca} > (i^*_{Ca} + HB_{ia-new})$, the upper switch is ON and the lower switch is OFF for leg "*a*". If $i_{Ca} < (i^*_{Ca} - HB_{ia-new})$, the upper switch is OFF and the lower switch is ON for leg "*a*". Similarly, for leg "*b*" and leg "*c*".

3.3. Design of an adaptive fixed-frequency hysteresis band controller for series inverter

Following a similar approach to the adaptive fixed-frequency hysteresis current controller in section 3.2, the expression for determining the bandwidth is given as follows:

$$HB_{va} = \frac{V_{dc}}{4 f_{sw} L_{Sa}} \left[1 - \frac{L^2_{Sa}}{V^2_{dc}} \left(\frac{d_{v^*_{Ca}}}{dt} + \frac{v_{Sa}}{L_{Sa}} \right)^2 \right] \tag{15}$$

Equation (15) shows that HB_v depends on the parameters f_{sw}, V_{dc}, L_{Sa}, v^*_{Ca}, and v_{Sa}. The DC-link voltage is stabilized using the fuzzy–PI controller as described in section 3.1. A fuzzy adjustor is used to adjust HB_{va} to $HB_{va\text{-}new}$ (similar to section 3.2). Each $HB_{va\text{-}new}$ is combined with the reference voltages $v^*_{Ca}, v^*_{Cb}, v^*_{Cc}$ and actual voltages v_{Ca}, v_{Cb}, v_{Cc} to generate gate pulses for the series inverter switches. The S-Function is written according to the rule: If $v_{Ca} > (v^*_{Ca} + HB_{va-new})$, the upper switch is ON and the lower switch is OFF for leg "*a*". If $v_{Ca} < (v^*_{Ca} - HB_{va-new})$, the upper switch is OFF and the lower switch is ON for leg "*a*". Similarly, for leg "*b*" and leg "*c*".

4. Simulation, experimental results, and discussion

4.1. Simulation results

To demonstrate the harmonic-mitigation effectiveness of the UPQC, simulations and experiments are conducted on the UPQC model shown in Figure 1 with two scenarios. In Scenario 1, a conventional proportional integral (PI) controller is used for DC-link voltage regulation, and traditional hysteresis band controls are used to control for both the series and shunt inverters. In Scenario 2, a fuzzy-PI controller is applied for DC-link voltage regulation, along with an adaptive fixed-frequency hysteresis band control for both the series and shunt inverters.

The UPQC parameters are given in Table 3.

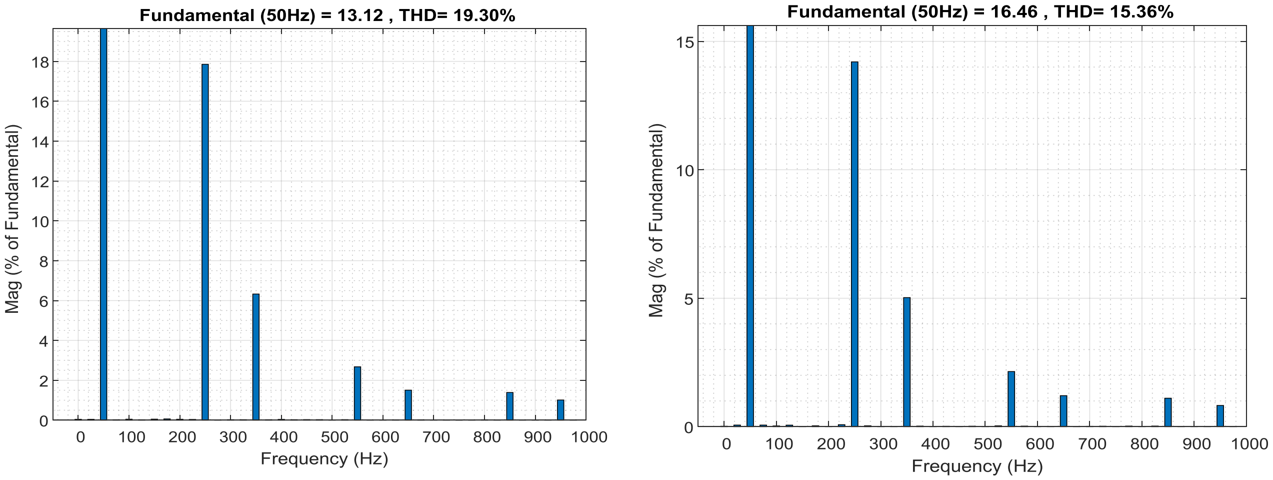
Table 3. UPQC parameters.

Source	380 V$_{\text{-rms;}}$ 50 Hz
Output filter of the shunt inverter	1 mH
Output filter of the series inverter	3.6 mH
DC-link capacitance	10000 µF
Reference DC-link voltage	700 V

The source voltage used in the simulations is defined as follows: from 0 to 0.2 s, the source is ideal. From 0.2 to 0.4 s, the source is ideal but swell. From 0.4 to 0.6 s, the source is ideal but sag. From

0.6 to 0.8 s, the source is unbalanced and distorted 10%. From 0.8 to 1.0 s, the source is ideal. From 1.0 to 1.2 s, the source is ideal but sag. From 1.2 to 1.4 s, the source is unbalanced and distorted 10%.

The frequency spectrum of the load current is shown in Figure 12. From 0 to 0.8 s, total harmonic distortion (THD) of the load current is 19.3%, as shown in Figure 12a. From 0.8 to 1.4 s, the load changes. THD of the load current is 15.36%, as shown in Figure 12b. The magnitude of the load harmonic components is shown in Table 4.



(a) (b)

Figure 12. Frequency spectrum of the load current; (a) from 0 to 0.8 s; (b) from 0.8 to 1.4 s.

Table 4. Magnitude of the load current harmonic components.

Frequency (Hz)	Magnitude (% of fundamental)	
	0–0.8 s	0.8–1.4 s
250	17.9	14.3
350	6.4	5.0
550	2.7	2.2
650	1.5	1.3
850	1.49	1.2
950	1.0	0.8

The waveforms to consider include three-phase source voltage, three-phase load current, three-phase supply current, three-phase load voltage, and DC-link voltage. The responses of UPQC in Scenario 1 are shown in Figure 13; when the three-phase source voltage or three-phase load current changes, the voltage on the DC-link changes.

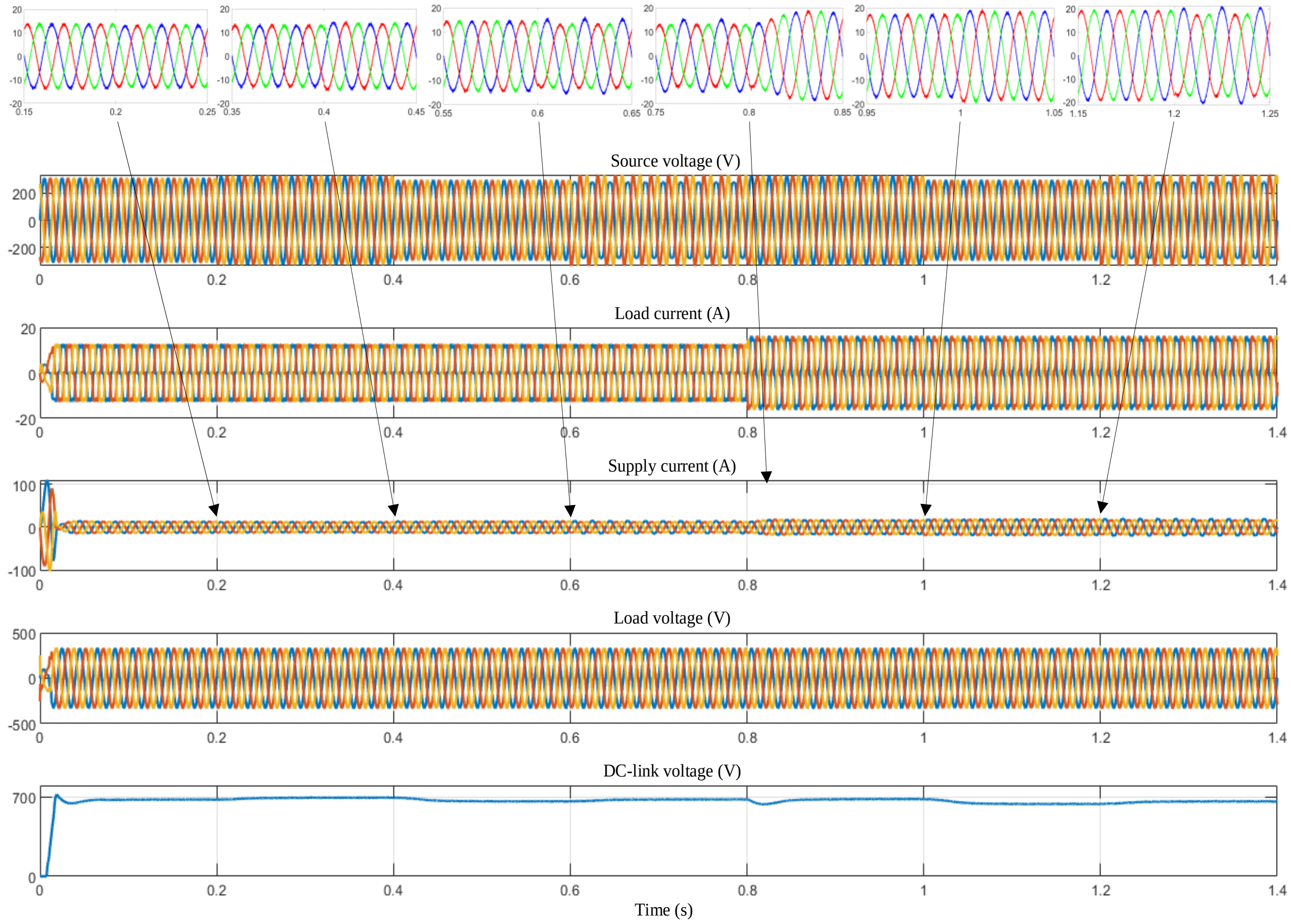
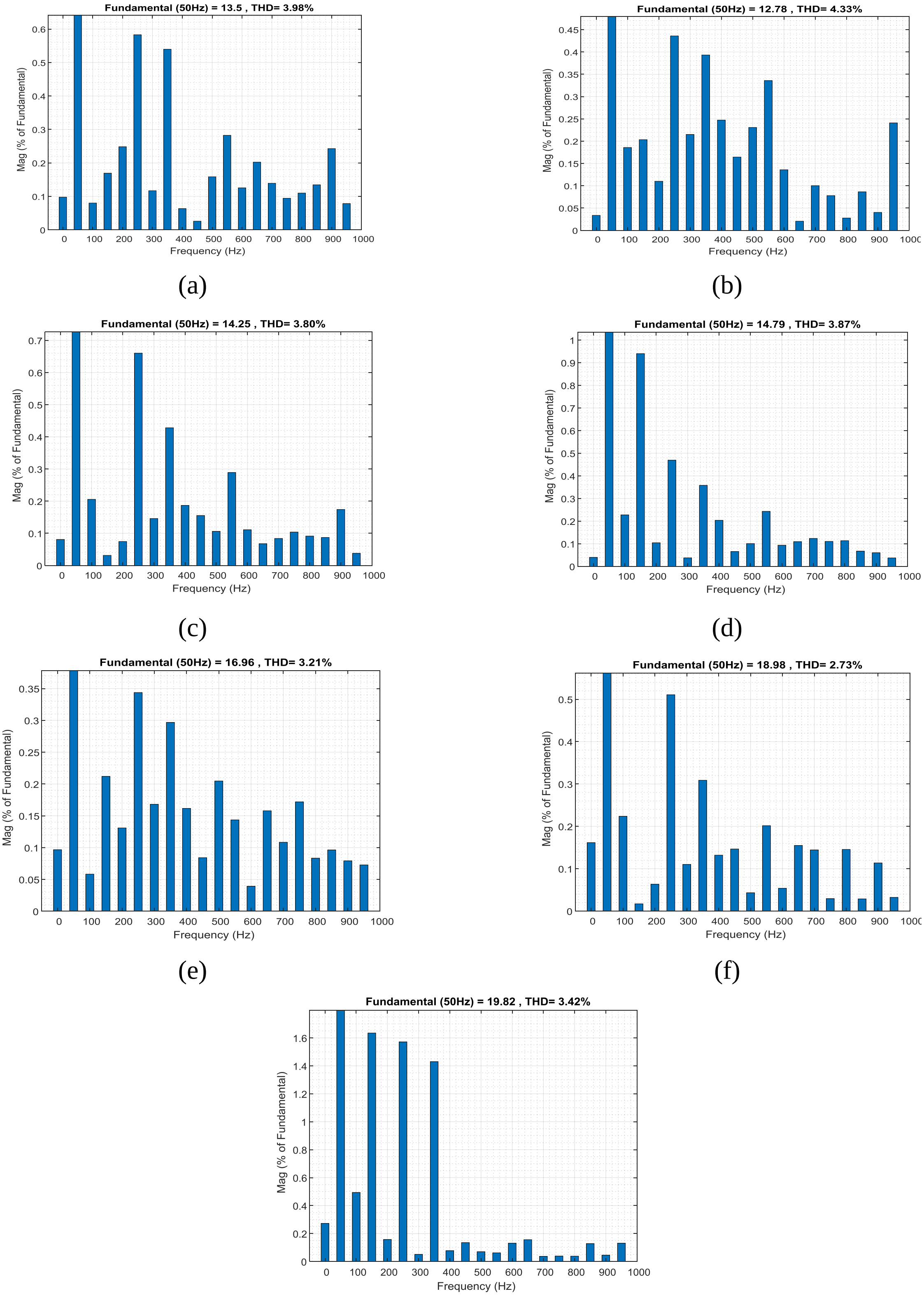


Figure 13. Responses of UPQC for Scenario 1.

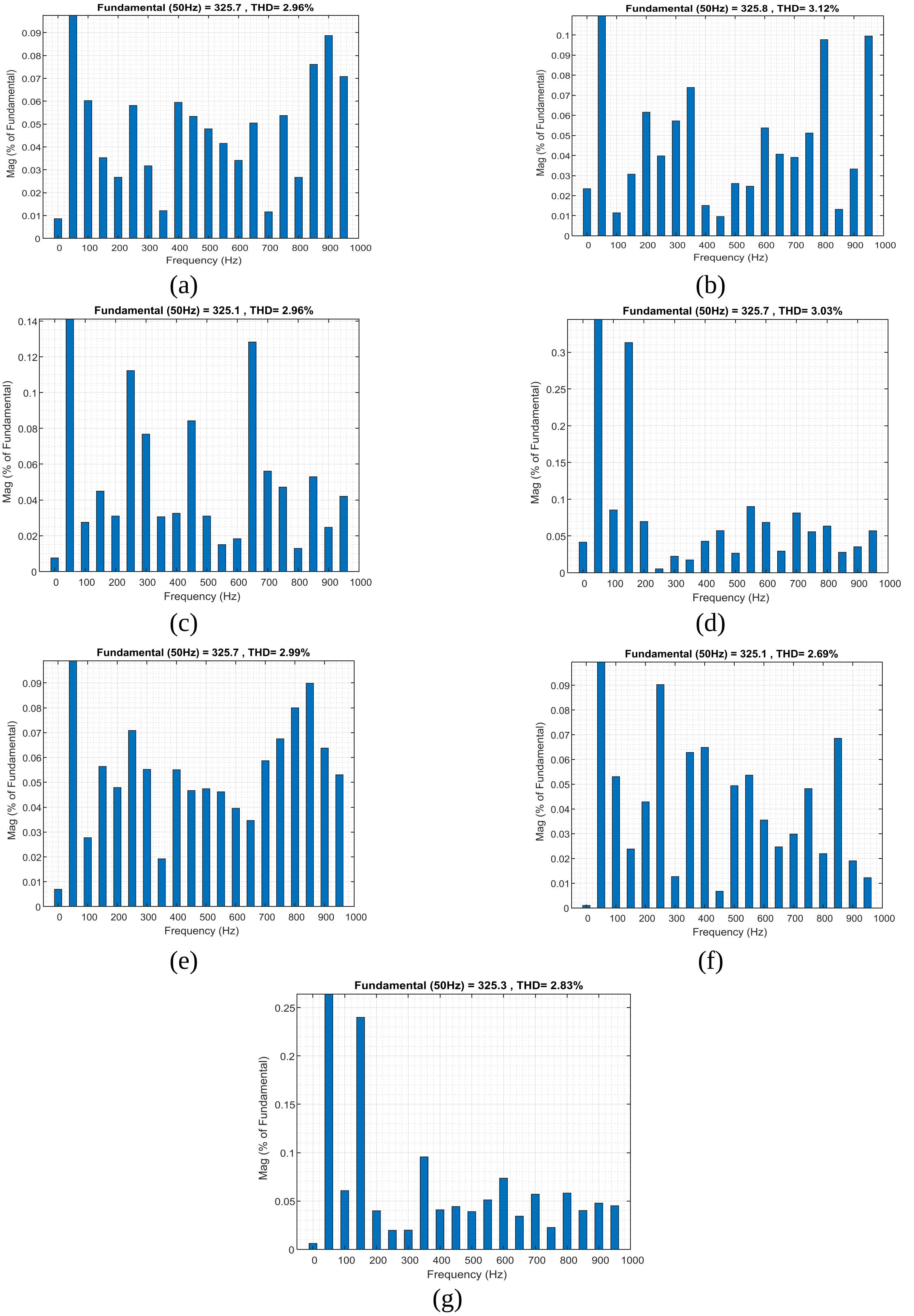
From Figure 13, the frequency spectrum of the supply current at steady state corresponds to the time intervals obtained as shown in Figures 14. The frequency spectrum of the load voltage at steady state corresponds to the time intervals obtained as shown in Figures 15. Simulation results from Figures 14 and 15 show that in the time interval from 0 to 0.8 s, the THD of the supply current decreases from 19.3% to less than 5%, and the THD of the load voltage is kept below 5%; especially, the fundamental component of the load voltage is kept stable at 325 V. In the time interval from 0.8 to 1.4 s, the load changes, the THD of the supply current decreases from 15.36% to less than 4%, and the THD of the load voltage is kept below 3%; especially, the fundamental component of the load voltage is kept stable at 325 V.

Thus, when Scenario 1 is used, the THD of the supply current and the THD of the load voltage are both less than 5%. Therefore, it satisfies the IEEE 519-2022 harmonic standard [29].



(a) (b) (c) (d) (e) (f) (g)

Figure 14. Frequency spectrum of the supply current at steady state when using Scenario 1; (a) from 0 to 0.2 s; (b) from 0.2 to 0.4 s; (c) from 0.4 to 0.6 s; (d) from 0.6 to 0.8 s; (e) from 0.8 to 1.0 s; (f) from 1.0 to 1.2 s; (g) from 1.2 to 1.4 s.



(a)

(b)

(c)

(d)

(e)

(f)

(g)

Figure 15. Frequency spectrum of the load voltage at steady state when using Scenario 1; (a) from 0 to 0.2 s; (b) from 0.2 to 0.4 s; (c) from 0.4 to 0.6 s; (d) from 0.6 to 0.8 s; (e) from 0.8 to 1.0 s; (f) from 1.0 to 1.2 s; (g) from 1.2 to 1.4 s.

The responses of UPQC in Scenario 2 are shown in Figure 16.

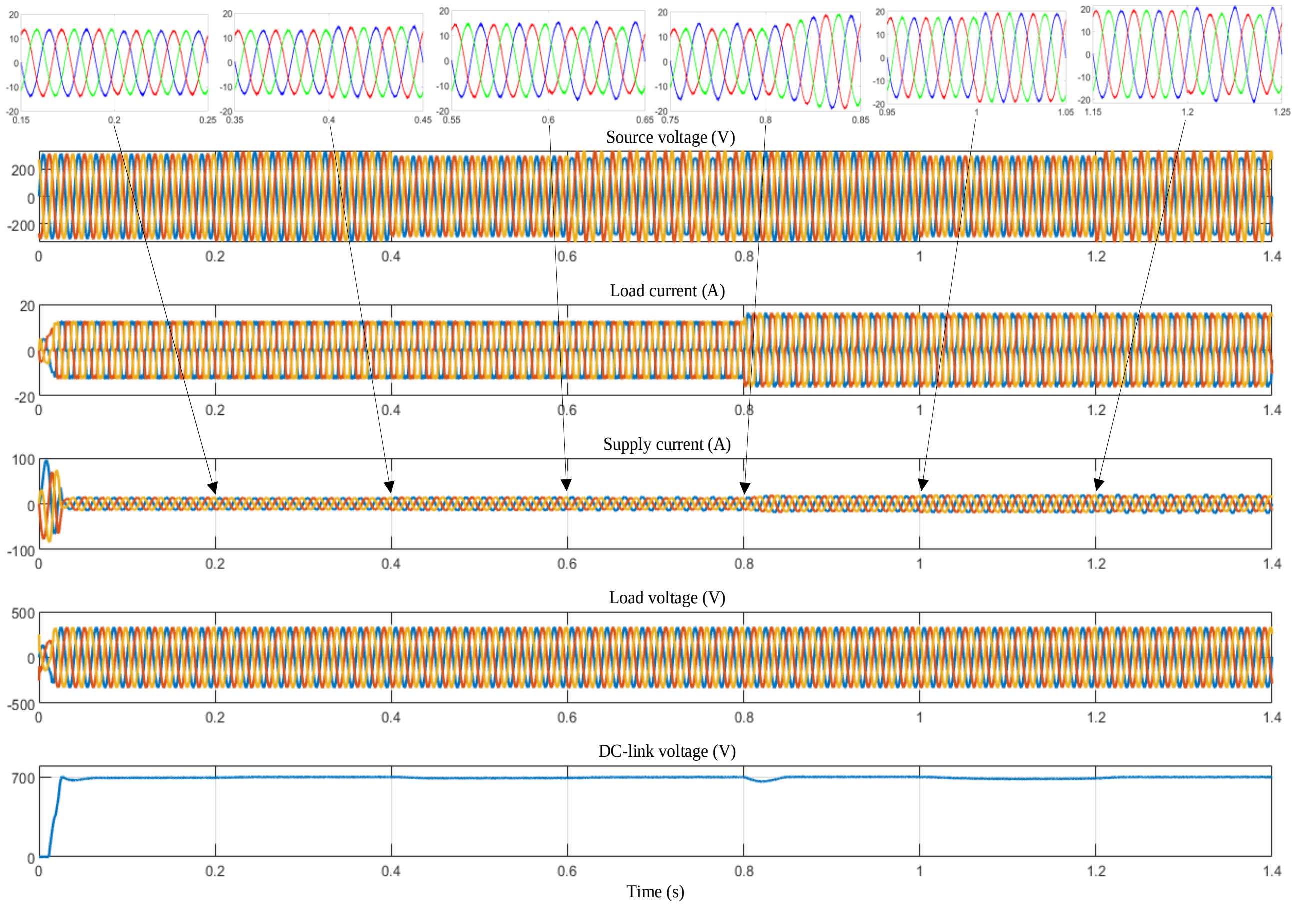
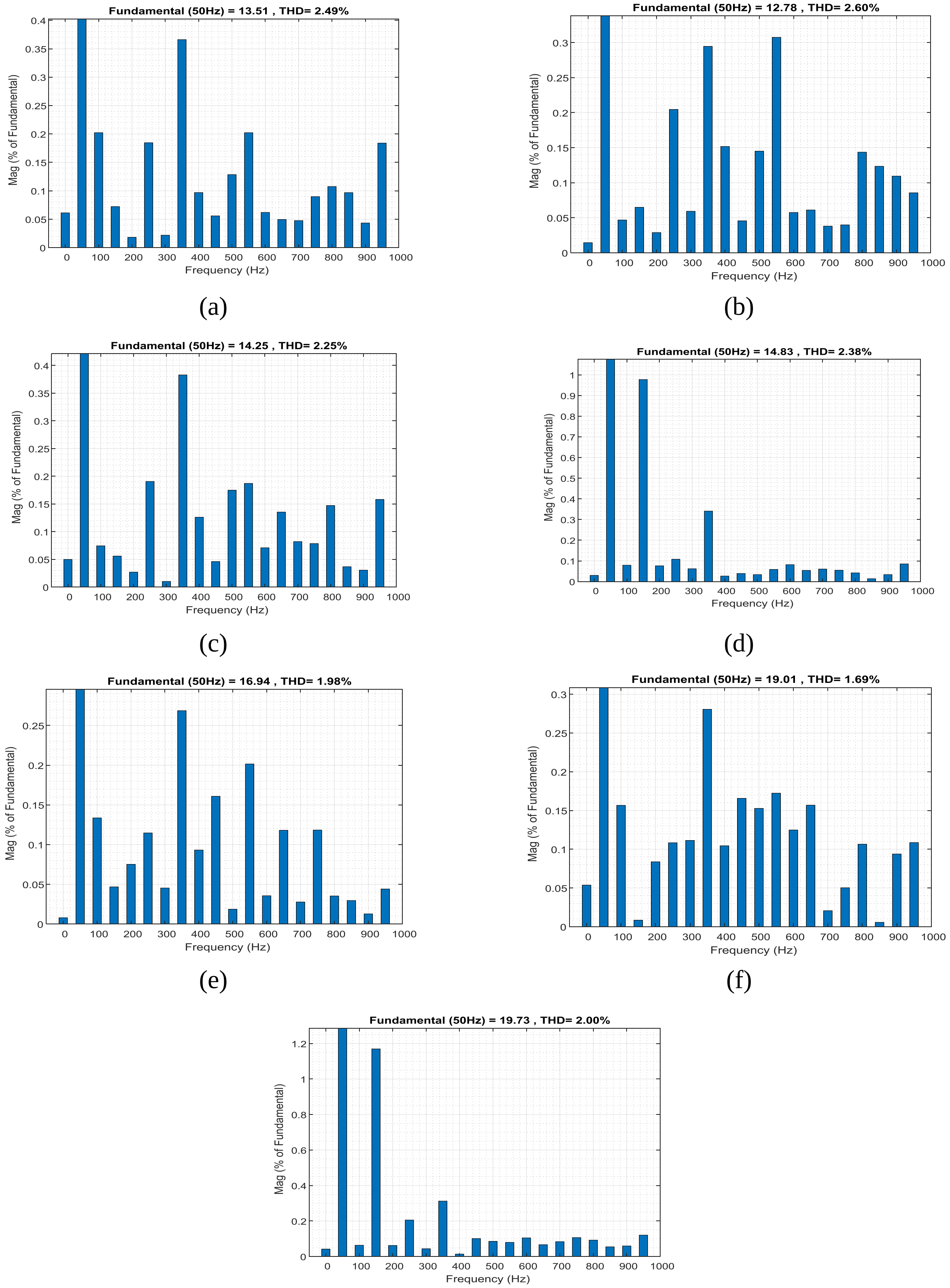


Figure 16. Responses of UPQC when using Scenario 2.

Figure 16 shows that, with Scenario 2, when the source voltage or load current changes, the DC-link voltage remains stable due to the use of a fuzzy-PI controller. Compared to Scenario 1, Scenario 2 shows a lower overshoot on the DC-link voltage waveform, shorter adjustment time, and smaller steady-state error. Only at time t = 0.8 s, when the source voltage and load current change simultaneously, the DC-link voltage drops significantly, but it quickly returns to the steady-state value of 700 V. This directly affects the performance of UPQC, specifically by significantly reducing the total harmonic distortion of the source current and load voltage and contributing to less switching frequency fluctuation.

In Figure 16, the frequency spectrum of the supply current and load voltage at steady state corresponds to the time intervals obtained as shown in Figures 17 and 18. Results from Figures 17 and 18 show that from 0 to 0.8 s, the THD of the supply current decreases from 19.3% to less than 3%, and the THD of the load voltage is kept below 2.3%; especially, the fundamental component of the load voltage is kept stable at 325 V. From 0.8 to 1.4 s, the load changes, the THD of the supply current decreases from 15.36% to less than 2%, and the THD of the load voltage is approximately 2%; especially, the fundamental component of the load voltage is kept stable at 325 V. Thus, when Scenario 2 is used, the THD of the supply current and the THD of the load voltage are both less than 5%. Therefore, it satisfies the IEEE 519-2022 harmonic standard [29].



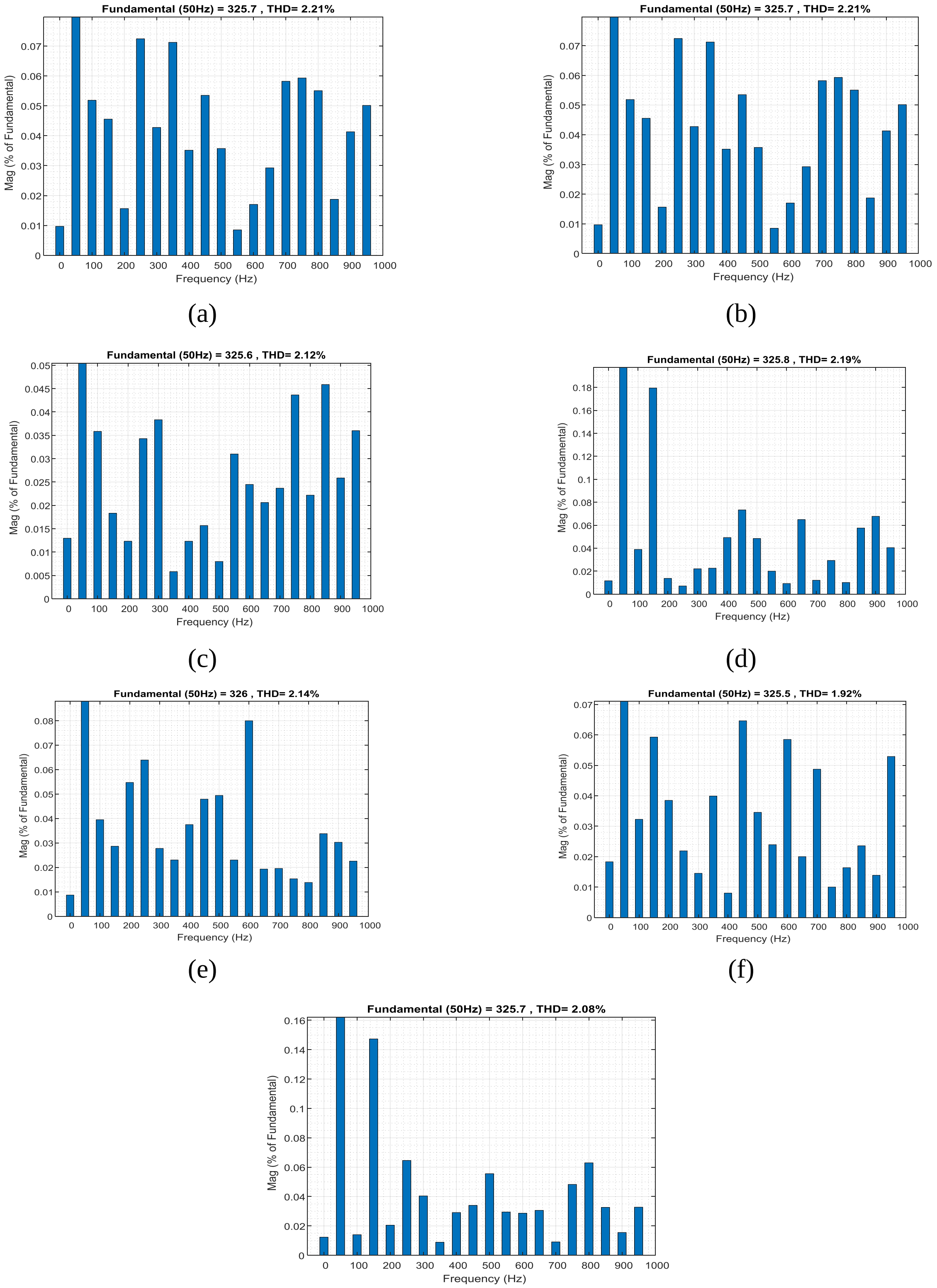
(a) (b)

(c) (d)

(e) (f)

(g)

Figure 17. Frequency spectrum of the supply current at steady state when using Scenario 2; (a) from 0 to 0.2 s; (b) from 0.2 to 0.4 s; (c) from 0.4 to 0.6 s; (d) from 0.6 to 0.8 s; (e) from 0.8 to 1.0 s; (f) from 1.0 to 1.2 s; (g) from 1.2 to 1.4 s.



(a)

(b)

(c)

(d)

(e)

(f)

(g)

Figure 18. Frequency spectrum of the load voltage at steady state when using Scenario 2; (a) from 0 to 0.2 s; (b) from 0.2 to 0.4 s; (c) from 0.4 to 0.6 s; (d) from 0.6 to 0.8 s; (e) from 0.8 to 1.0 s; (f) from 1.0 to 1.2 s; (g) from 1.2 to 1.4 s.

From the results obtained in Figures 14 and 17, a comparison of the magnitudes of the harmonic components of the supply current for the two scenarios is shown in Table 5.

Table 5. Comparison of the magnitude of the harmonic components of the supply current for two scenarios.

Scenarios	Times	Magnitude of the harmonic components (% of fundamental)						THD of the supply current at steady state (%)
		5th	7th	11th	13th	17th	19th	
Scenario 1	0–0.2 s	0.58	0.54	0.28	0.2	0.14	0.08	3.98
	0.2–0.4 s	0.44	0.39	0.345	0.02	0.08	0.24	4.33
	0.4–0.6 s	0.66	0.43	0.29	0.07	0.09	0.03	3.80
	0.6–0.8 s	0.47	0.36	0.24	0.11	0.07	0.04	3.87
	0.8–1.0 s	0.34	0.29	0.14	0.17	0.09	0.07	3.21
	1.0–1.2 s	0.52	0.32	0.2	0.16	0.03	0.04	2.73
	1.2–1.4 s	1.57	1.46	0.55	0.18	0.12	0.12	3.42
Scenario 2	0–0.2 s	0.18	0.36	0.2	0.05	0.09	0.18	2.49
	0.2–0.4 s	0.2	0.29	0.31	0.06	0.12	0.08	2.60
	0.4–0.6 s	0.18	0.38	0.18	0.13	0.03	0.16	2.25
	0.6–0.8 s	0.1	0.35	0.05	0.05	0.02	0.08	2.38
	0.8–1.0 s	0.12	0.27	0.2	0.12	0.03	0.04	1.98
	1.0–1.2 s	0.11	0.28	0.18	0.16	0.01	0.11	1.69
	1.2–1.4 s	0.2	0.31	0.09	0.07	0.05	0.12	2.0

Table 6. Comparison of the magnitude of the harmonic components of the load voltage for two scenarios.

Scenarios	Times	Magnitude of the harmonic components (% of fundamental)						THD of the load voltage at steady state (%)
		5th	7th	11th	13th	17th	19th	
Scenario 1	0–0.2 s	0.058	0.032	0.042	0.05	0.076	0.07	2.96
	0.2–0.4 s	0.04	0.075	0.025	0.04	0.014	0.1	3.12
	0.4–0.6 s	0.11	0.03	0.018	0.13	0.055	0.042	2.96
	0.6–0.8 s	0.01	0.02	0.08	0.03	0.03	0.06	3.03
	0.8–1.0 s	0.07	0.02	0.045	0.035	0.09	0.052	2.99
	1.0–1.2 s	0.09	0.063	0.055	0.025	0.068	0.012	2.69
	1.2–1.4 s	0.02	0.09	0.05	0.03	0.03	0.04	2.83
Scenario 2	0–0.2 s	0.072	0.071	0.009	0.028	0.018	0.05	2.21
	0.2–0.4 s	0.072	0.071	0.008	0.028	0.018	0.05	2.21
	0.4–0.6 s	0.034	0.006	0.031	0.021	0.045	0.035	2.12
	0.6–0.8 s	0.006	0.022	0.02	0.062	0.05	0.04	2.19
	0.8–1.0 s	0.065	0.023	0.023	0.02	0.035	0.023	2.14
	1.0–1.2 s	0.022	0.04	0.024	0.02	0.024	0.059	1.92
	1.2–1.4 s	0.062	0.008	0.03	0.032	0.035	0.035	2.08

The data from Table 5 shows that in each time interval, the magnitude of the 5th, 7th, 11th, 13th, 17th, and 19th harmonic components decreased significantly when using Scenario 2 compared to when using Scenario 1. The THD of the supply current at steady state in each time interval when using Scenario 2 was also lower than when using Scenario 1. This proves that Scenario 2 is more effective than Scenario 1 in reducing the magnitude of harmonic components and reducing the THD of the supply current.

From the results obtained in Figures 15 and 18, a comparison of the magnitudes of the harmonic components of the load voltage for the two scenarios is shown in Table 6.

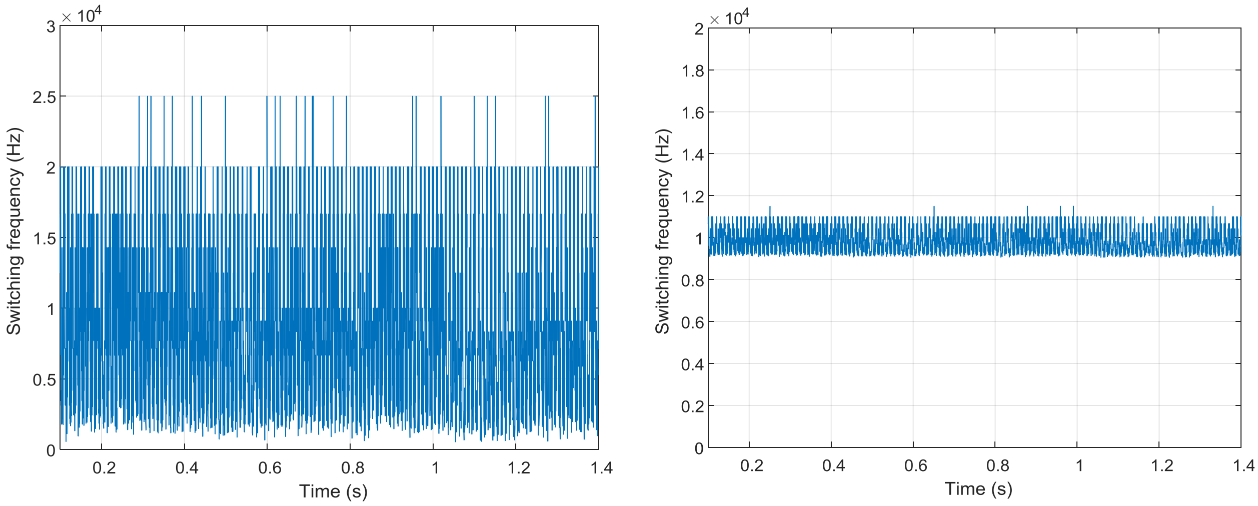
The data in Table 6 shows that within each time interval, the magnitudes of the order 5th, 7th, 11th, 13th, 17th, and 19th load voltage harmonics in the two scenarios alternate between large and small values. However, according to Figure 16, in addition to the harmonics listed above, many other harmonics with fairly large amplitudes also appear, such as the orders 3rd, 9th, 12th, and 16th. Despite this, the THD of the load voltage for each time interval when using Scenario 2 is lower than when using Scenario 1, and the change in THD for the time intervals when using Scenario 2 is also more stable (from 1.92% to 2.21%) than when using Scenario 1 (from 2.69% to 3.12%). This demonstrates that Scenario 2 is more effective than Scenario 1 in reducing the THD of the load voltage in each time interval.

From the DC-link voltage waveforms in Figures 13 and 16, a comparison of DC-link voltage stability for the two scenarios is shown in Table 7. According to Table 7, in the time interval from 0 to 0.2 s, the overshoot is 23 V (compared to 700 V) for Scenario 1, and 2.5 V (compared to 700 V) for Scenario 2; there is no overshoot in the remaining time intervals. The regulation time when using Scenario 2 is smaller than when using Scenario 1 in all time intervals. The steady-state error when using Scenario 2 is also much smaller than when using Scenario 1 in all time intervals. This demonstrates that when the source and load change, the DC-link voltage when using Scenario 2 is better than when using Scenario 1 in reducing overshoot, regulation time, and steady-state error.

Table 7. Comparison of DC-link voltage stability for two scenarios.

Scenarios	Times	Overshoot (V)	Regulation time (s)	Steady-state error (V)
Scenario 1	0–0.2 s	23	0.08	24
	0.2–0.4 s	0	0.05	6
	0.4–0.6 s	0	0.07	20
	0.6–0.8 s	0	0.06	24
	0.8–1.0 s	0	0.08	20
	1.0–1.2 s	0	0.08	63
	1.2–1.4 s	0	0.08	20
Scenario 2	0–0.2 s	2.5	0.065	5
	0.2–0.4 s	0	0.03	0
	0.4–0.6 s	0	0.04	10
	0.6–0.8 s	0	0.02	0
	0.8–1.0 s	0	0.05	0
	1.0–1.2 s	0	0.06	17
	1.2–1.4 s	0	0.06	0

The results of comparing the switching frequency of the semiconductor switch of the inverter corresponding to the two scenarios are shown in Figure 19. Figure 19a shows that when using Scenario 1 (traditional hysteresis control), the switching frequency changes greatly, whereas with Scenario 2 (adaptive fixed-frequency hysteresis band control), the switching frequency fluctuates much less (oscillating around the reference frequency of 10 kHz), as shown in Figure 19b. This is very useful for designing the output filters for the inverter in UPQC.



(a) (b)

Figure 19. Switching frequency of the semiconductor switch in the inverter; (a) using Scenario 1; (b) using Scenario 2.

4.2. Experimental results

To demonstrate the practical feasibility of the proposed method, experiments were conducted using a Hardware-In-the-Loop (HIL) control loop with a real-time lab, as shown in Figure 20. In this arrangement, the UPQC system and its control algorithm are executed directly on the OP5707XG real-time simulator. The OP5330 card handles the plant-side signals, while the OP5340 card is assigned to the controller-side functions. A host computer equipped with MATLAB/Simulink and RT-Lab is used only for compilation, parameter tuning, and monitoring. The real-time simulator is equipped with 32 Intel® Xeon® 3.8 GHz CPUs, providing high-performance parallel computation, and an AMD Virtex™-7 485T FPGA, which enables high-speed signal processing and deterministic control tasks. Signal acquisition is carried out through OP5340 analog input modules, which capture the measured voltage and current signals from the UPQC system, while OP5330 analog output modules are responsible for generating analog control signals that drive the power electronic converters. The output of the UPQC is connected to the controller inputs via a DB-37 shielded cable, ensuring stable communication and reduced electromagnetic interference. The UPQC system model delivers analog signals such as source voltages (v_{Sa}, v_{Sb}, v_{Sc}), load voltages (v_{La}, v_{Lb}, v_{Lc}), the DC-link voltage (V_{dc}), and load currents (i_{La}, i_{Lb}, i_{Lc}). These inputs are processed by the control subsystem, which generates 12 PWM gating signals ($G1$–$G12$). The PWM outputs are then fed back to the inverter model, thereby closing the control loop in real time. The experimental parameters of the UPQC system are given in Table 3, with a scale voltage of 1/50, a scale current of 1/20, a sample time of 0.00001 s, and a switching frequency of 10 kHz.

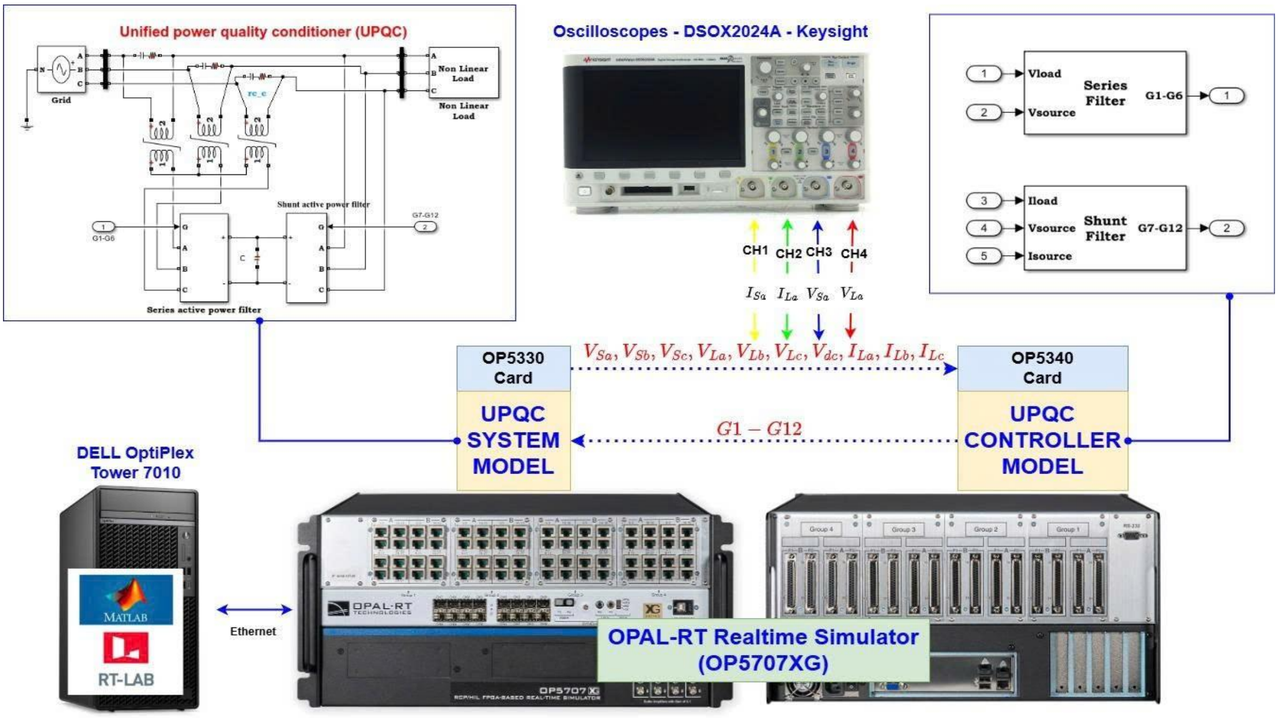


Figure 20. UPQC experimental configuration based on HIL.

Experimental results with Scenario 1 are shown in Figure 21, and the waveforms at the state transition points are magnified in Figure 22.

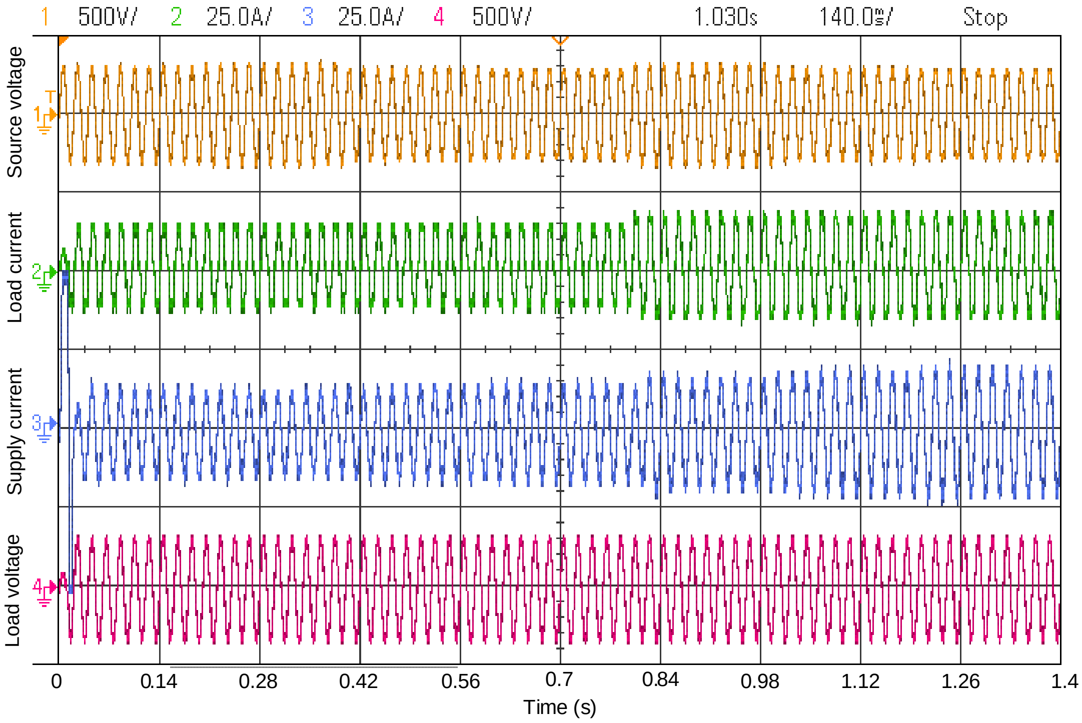
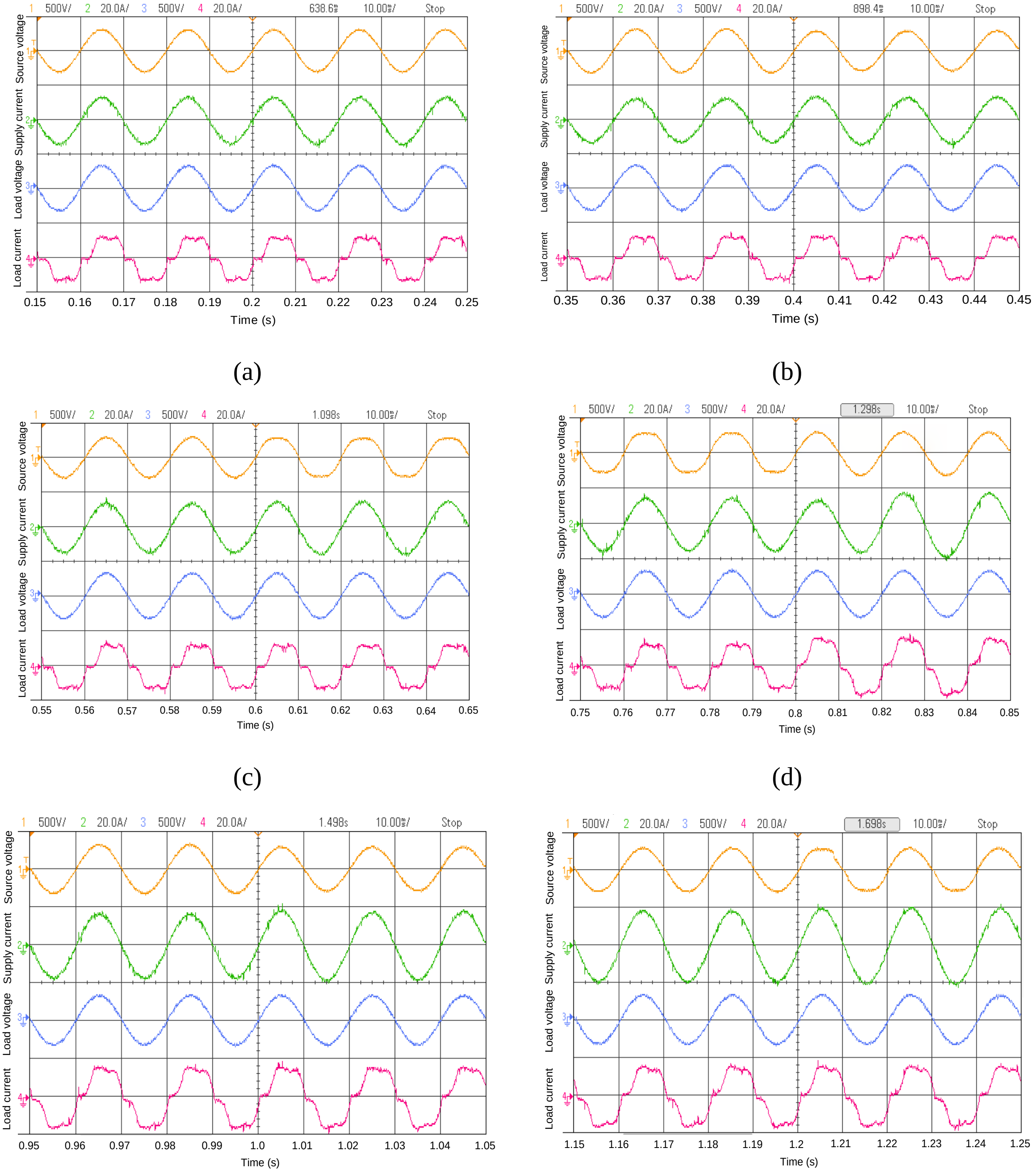


Figure 21. Experimental results with Scenario 1.



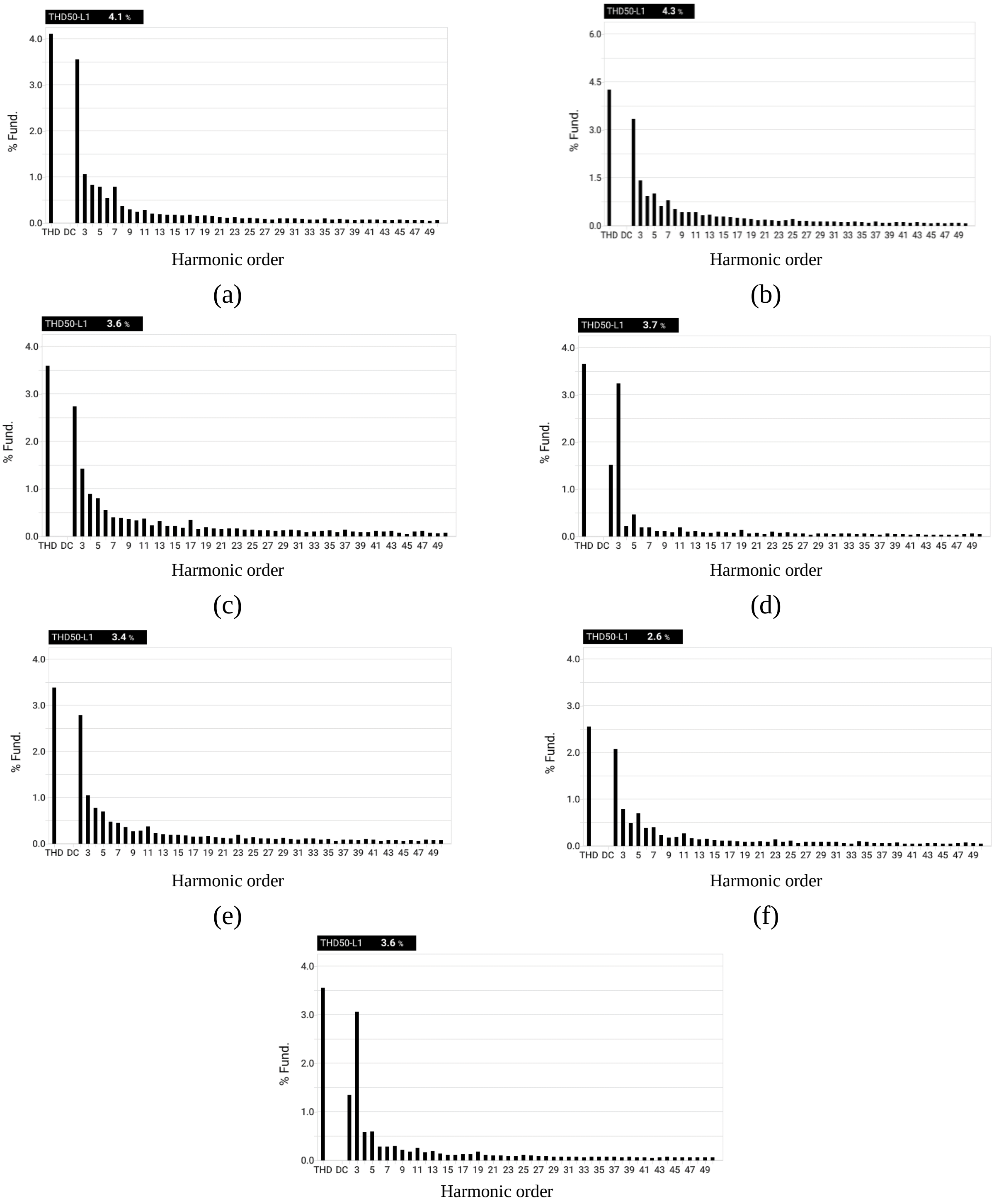
(a) (b)

(c) (d)

(e) (f)

Figure 22. Magnified experimental results at state transition points with Scenario 1; (a) increasing source voltage; (b) decreasing source voltage; (c) distorted source voltage; (d) ideal source voltage and changing load; (e) decreasing source voltage and changing load; (f) distorted source voltage and changing load.

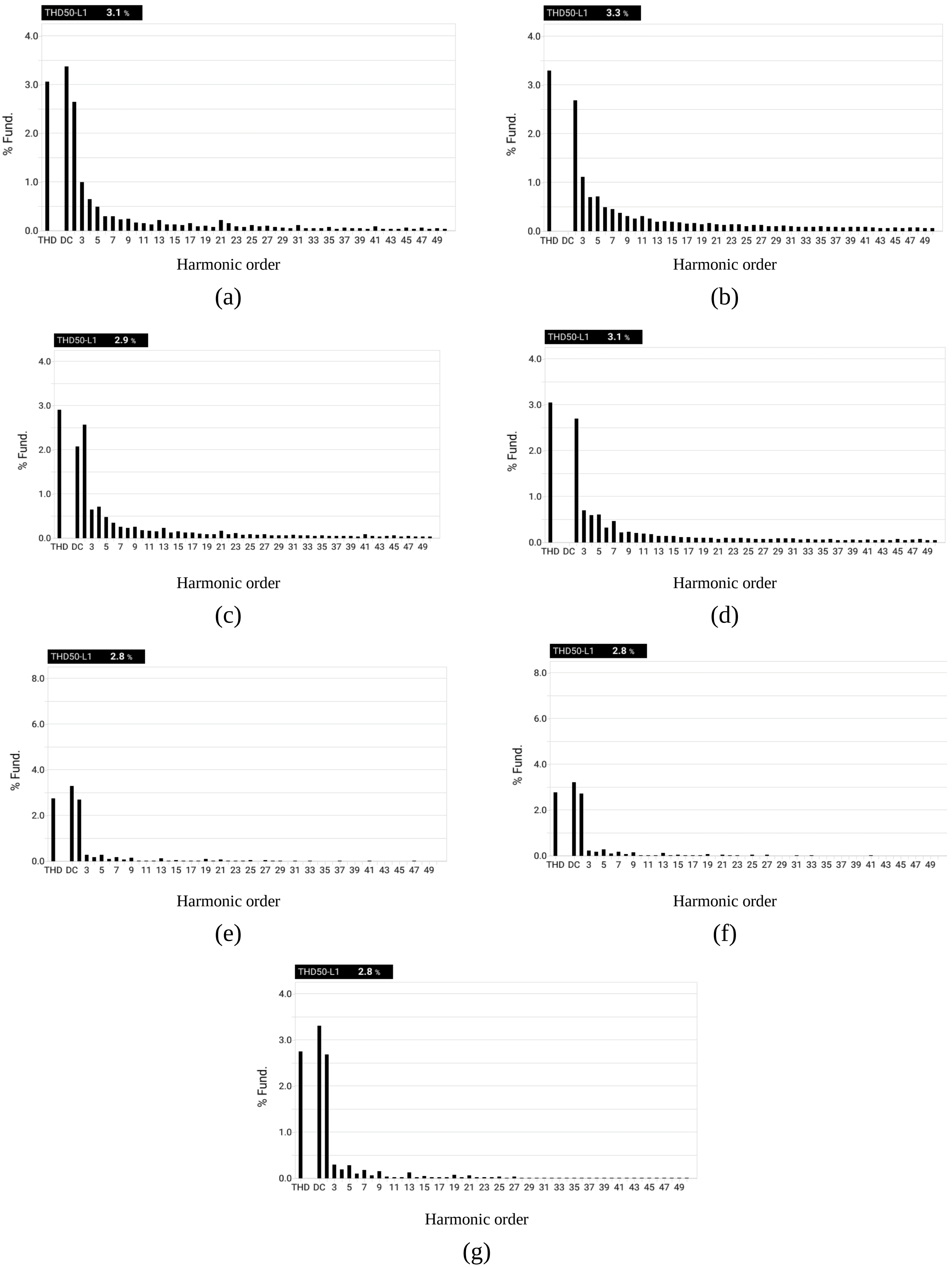
The frequency spectrum of the supply current at steady state when using Scenario 1 is shown in Figure 23.



(a) (b) (c) (d) (e) (f) (g)

Figure 23. Frequency spectrum of the supply current at steady state when using scenario 1; (a) 0–0.2 s; (b) 0.2–0.4 s; (c) 0.4–0.6 s; (d) 0.6–0.8 s; (e) 0.8–1.0 s; (f) 1.0–1.2 s; (g) 1.2–1.4 s.

The frequency spectrum of the load voltage at steady state when using Scenario 1 is shown in Figure 24.



(a) (b) (c) (d) (e) (f) (g)

Figure 24. Frequency spectrum of load voltage at steady state when using Scenario 1; (a) 0–0.2 s; (b) 0.2–0.4 s; (c) 0.4–0.6 s; (d) 0.6–0.8 s; (e) 0.8–1.0 s; (f) 1.0–1.2 s; (g) 1.2–1.4 s.

Experimental results with Scenario 2 are shown in Figure 25, and the waveforms at the state transition points are magnified in Figure 26.

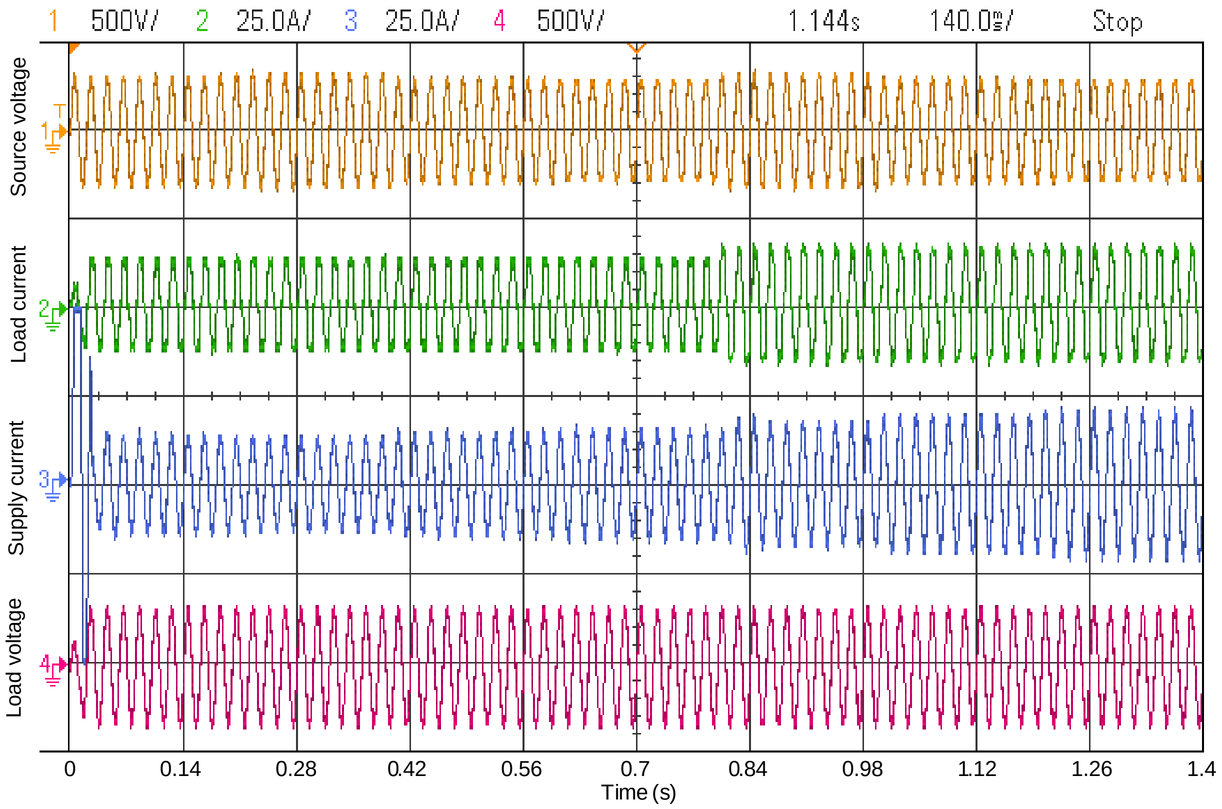


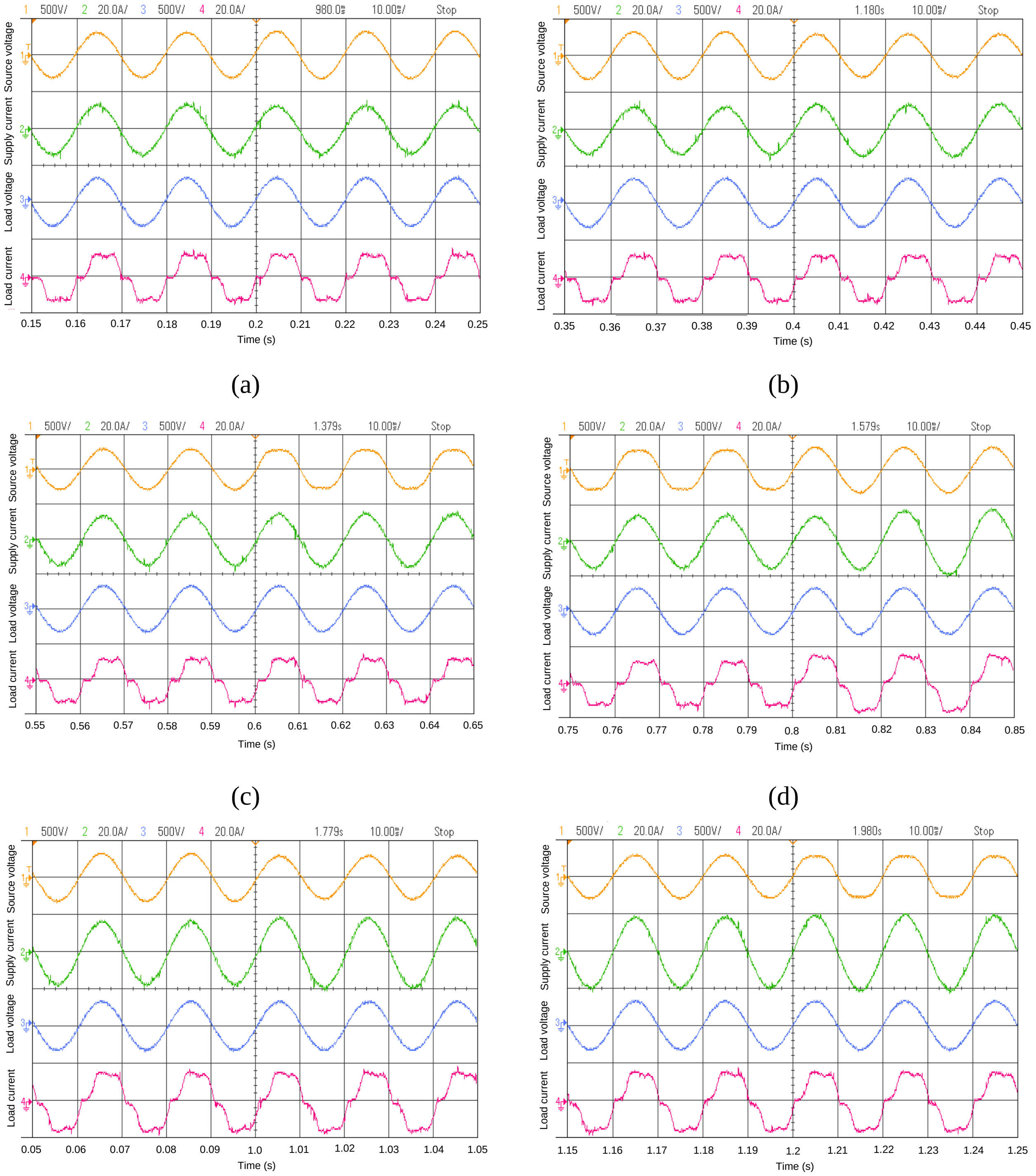
Figure 25. Experimental results with Scenario 2.

The frequency spectrum of the supply current at steady state when using Scenario 2 is shown in Figure 27; the frequency spectrum of the load voltage at steady state when using Scenario 2 is shown in Figure 28.

A comparison of the THD of the supply current and load voltage for the two scenarios is summarized in Table 8. DC-link voltage waveforms when using Scenarios 1 and 2 are shown in Figure 29.

Figure 29 demonstrates that when using Scenario 2, the DC-link voltage has a smaller overshoot, shorter adjustment time, and smaller steady-state error than when using Scenario 1. Experimental results have proven that Scenario 2 is more effective than Scenario 1 in reducing supply current distortion, reducing load voltage distortion, and stabilizing the DC-link voltage.

From the experimental process, while the proposed scheme demonstrates superior performance in HIL simulations, several engineering limitations must be acknowledged for practical deployment. First, the high investment costs of the back-to-back converter and the series injection transformer remain a significant barrier compared to simpler solutions like shunt APF. Second, the hardware complexity is considerable; implementing adaptive control laws requires a digital signal processor and high-speed FPGA to maintain real-time determinism. Future work should explore transformerless configurations and reduced-sensor algorithms to mitigate these cost and complexity issues, enhancing the commercial viability of the UPQC.

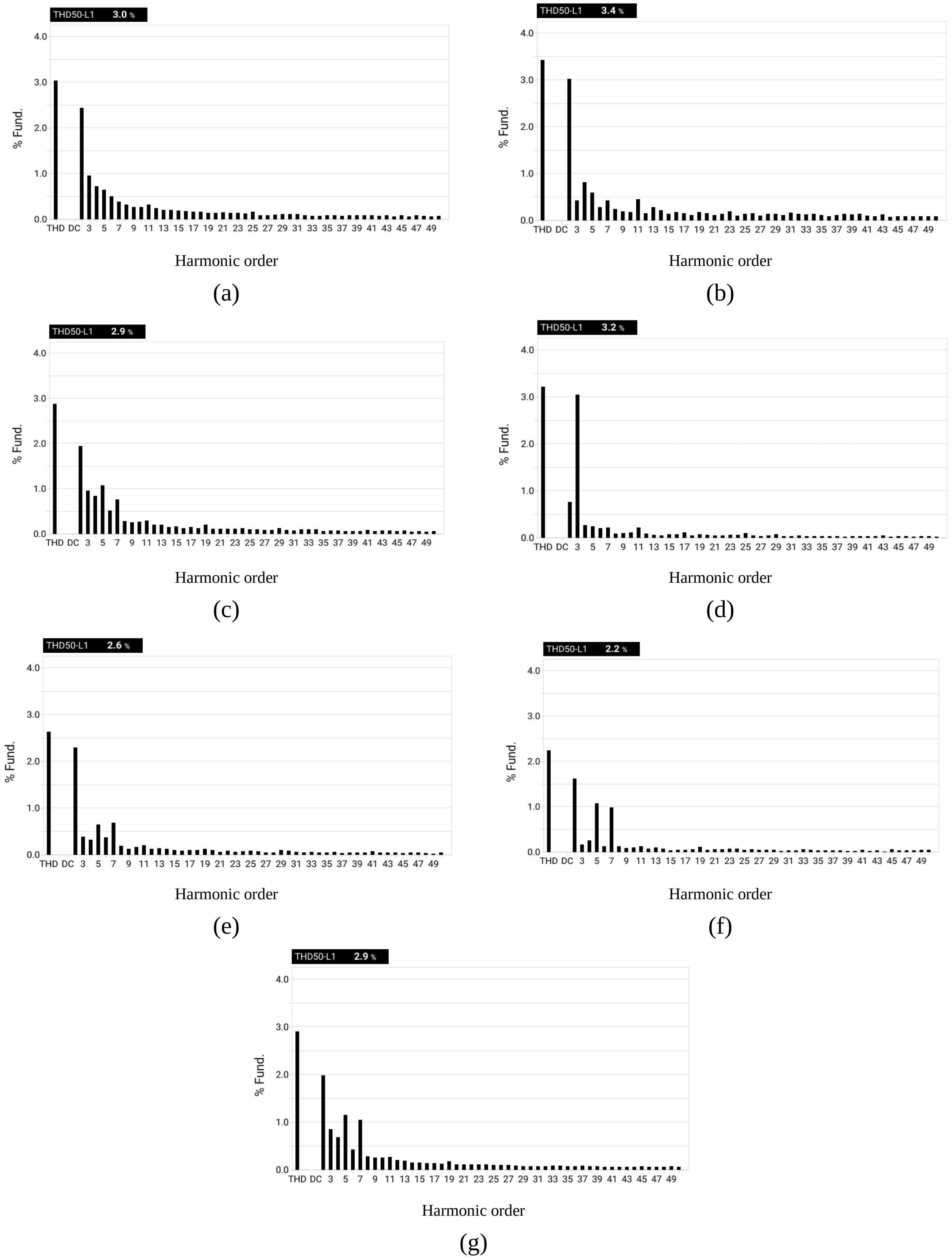


(a) (b)

(c) (d)

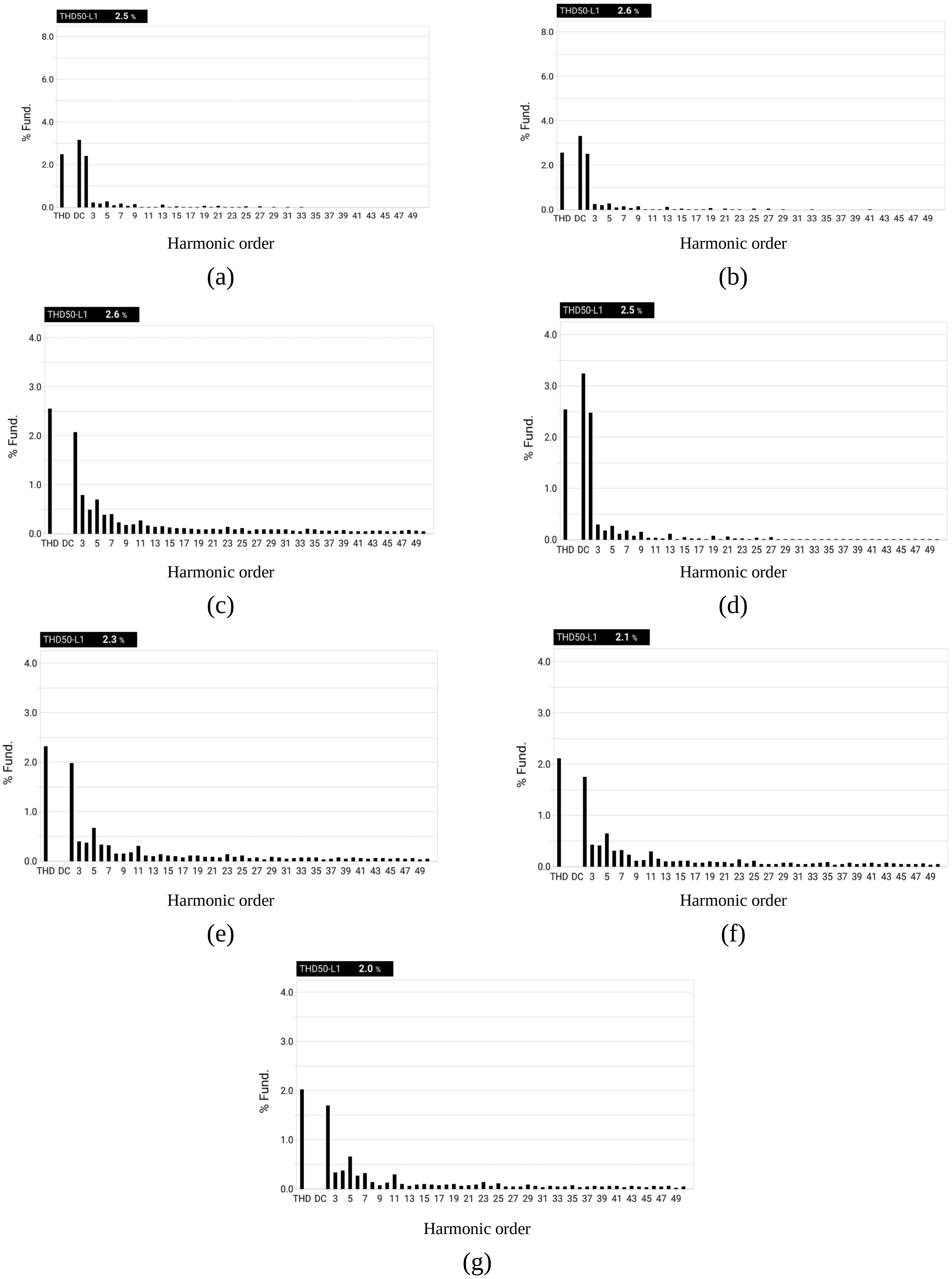
(e) (f)

Figure 26. Magnified experimental results at state transition points with Scenario 2; (a) increasing source voltage; (b) decreasing source voltage; (c) distorted source voltage; (d) ideal source voltage and changing load; (e) decreasing source voltage and changing load; (f) distorted source voltage and changing load.



(a) (b) (c) (d) (e) (f) (g)

Figure 27. Frequency spectrum of the supply current at steady state when using Scenario 2; (a) 0–0.2 s; (b) 0.2–0.4 s; (c) 0.4–0.6 s; (d) 0.6–0.8 s; (e) 0.8–1.0 s; (f) 1.0–1.2 s; (g) 1.2–1.4 s.



(a)

(b)

(c)

(d)

(e)

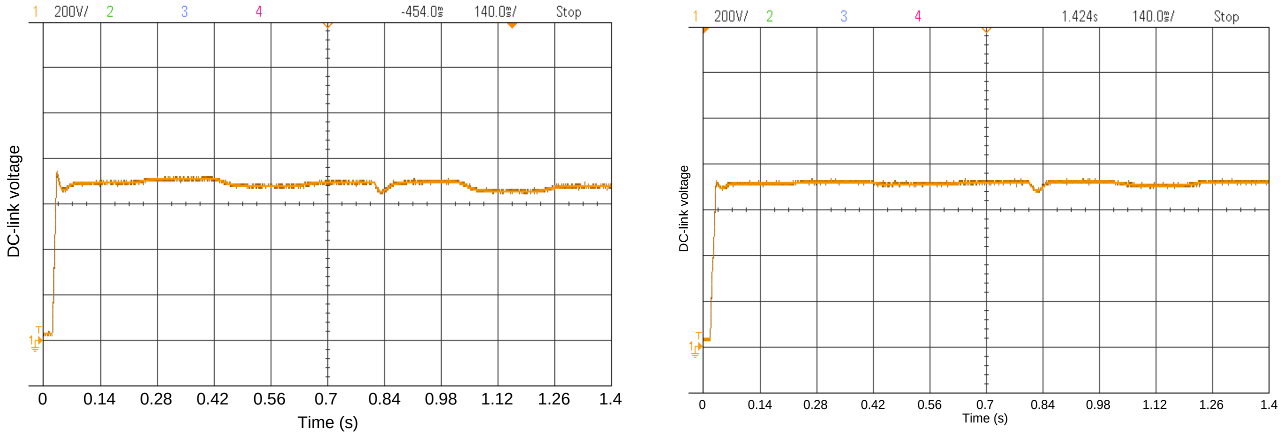
(f)

(g)

Figure 28. Frequency spectrum of the load voltage at steady state when using Scenario 2; (a) 0–0.2 s; (b) 0.2–0.4 s; (c) 0.4–0.6 s; (d) 0.6–0.8 s; (e) 0.8–1.0 s; (f) 1.0–1.2 s; (g) 1.2–1.4 s.

Table 8. Comparison of experimental results of the THD of the supply current and load voltage for two scenarios.

Scenarios	Times	THD of the supply current at steady state (%)	THD of the load voltage at steady state (%)
Scenario 1	0–0.2 s	4.1	3.1
	0.2–0.4 s	4.3	3.4
	0.4–0.6 s	3.6	2.9
	0.6–0.8 s	3.7	3.1
	0.8–1.0 s	3.4	2.8
	1.0–1.2 s	2.6	2.8
	1.2–1.4 s	3.6	2.8
Scenario 2	0–0.2 s	3.0	2.5
	0.2–0.4 s	3.4	2.6
	0.4–0.6 s	2.9	2.6
	0.6–0.8 s	3.2	2.5
	0.8–1.0 s	2.6	2.3
	1.0–1.2 s	2.2	2.1
	1.2–1.4 s	2.9	2.0



(a) (b)

Figure 29. DC-link voltage; (a) Scenario 1; (b) Scenario 2.

5. Conclusions

This paper presents a new control method for UPQC, namely the adaptive fixed-frequency hysteresis band control. First, the structure and mathematical control model of a UPQC are introduced. Methods for determining reference harmonic voltages and reference harmonic currents are also detailed. Based on this, a fuzzy-PI controller is applied to stabilize the DC-link voltage, and an adaptive fixed-frequency hysteresis band control method is developed for controlling shunt/series inverters. Simulations and experiments were conducted for two scenarios with varying source voltage and load conditions: Scenario 1 uses a traditional PI controller to stabilize the DC-link voltage and a traditional hysteresis controller to control shunt/series inverters, and Scenario 2 uses a fuzzy-PI controller to stabilize the DC-link voltage and an adaptive fixed-frequency hysteresis band control to control shunt/series inverters. The results demonstrated that Scenario 2 was more effective than Scenario 1 in reducing the THD of the supply current, reducing the THD of the load voltage, and stabilizing the DC-link voltage. Furthermore, in Scenario 2, the bandwidth is adjusted to maintain a constant switching frequency, which is very useful in designing the output filters of the UPQC.

Author contributions

Nguyen Duc Toan: Software, investigation, writing—original draft, project administration, funding acquisition. Chau Minh Thuyen: Conceptualization, methodology, formal analysis, resources, writing—review and editing, supervision, funding acquisition. Tran Tan Tai: validation, data curation, visualization. All authors have read and agreed to the published version of the manuscript.

Use of Generative-AI tools declaration

The authors declare they have not used Artificial Intelligence (AI) tools in the creation of this article.

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Conflict of interest

The authors declare that they have no conflicts of interest in this paper.

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