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*Research article*

# Implementation of on-chip high precision oscillators with RC and LC using digital compensation technique

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**Abstract:** High precision oscillators became a significant call for both designer and testing engineers. Modern vibrators are being utilized in a variety of circuits, and accessibility to a wide range of frequencies is of the utmost importance in all research establishments. To produce various frequencies, utilizing a single gadget is very challenging for the designers. This article aims to provide the low frequency (RC) oscillator and high frequency (LC) oscillators with various output frequencies on a single chip. The use of both oscillators is necessary due to the fact that there are currently no such devices on the market, which makes it necessary to avoid using bulky recurrence generator hardware in order to facilitate rapid exploration and plausibility research. Here, a RC oscillator with high current accuracy and a LC oscillator with low force have been used to design a voltage controlled oscillator (VCO) IC by utilizing the Cadence 45 nm technology. This particular VCO IC is able to obtain two different frequencies with reasonable precision. Further, execution is completed by utilizing exclusive requirement inconsistent message format designing. This proposed work can be used at both audio frequency and radio frequency ranges from megahertz (MHz) to gigahertz (GHz).

**Keywords:** voltage control oscillator; digital compensation technique, high precision oscillators; frequency

## 1. Introduction

In this research, we are primarily concerned with providing excellent and user-friendly medium-

and high-frequency generators on a single chip. We anticipated incorporating RC and LC oscillators with different frequencies on a single chip. On-chip prepares for the most part to demonstrate network characteristics such as force utilization, area, speed, and cost. The crucial characteristic of an RC oscillator is its repetition strength [1]. Consideration is given to the repeatability of temperature variations and supply voltage variations. In the past, a balancing crossing out plan was used, which reduced temperature strength at low power. A self-isolated oscillator is used for steady clock output. This has the disadvantages of susceptible stage upheaval and high reaction time as a result of restricted bandwidth. Traded capacitor aggregated data is utilized to construct the oscillator's tenacity and reduce the glimmer noise [2]. A complementary cross coupled topology can be used to reduce the phase noise contribution due to the current noise sources [3]. The phase noise also can also be removed by automatic level control circuitry (ALC) in the micro mechanical regenerators [4]. Higher power consumption and more areas are drawbacks of this method.

In previous research, the influence of compensation Frequency ($t_{comp}$) was reduced by varying the reference voltage in comparators using a technique known as voltage averaging input. The majority of basic integrator analysis circles employ these procedures to establish repetition sufficiency; nevertheless, it demands more power consumption. Ring oscillators repeat got circles. This may affect the benchmark. In FLL, a very low-power enhancer has an effect on the VCO when the temperature fluctuates. Feed forward approach in a detuned oscillator is used to reduce compensation frequency using a support charging scheme. Repeat pay systems can be used in similar manner. These strategies require more power. When designing an on-chip oscillator, it is difficult to ensure repeat stability against variations in temperature and voltage. Various types of resistors are used to reduce temperature coefficients [2]. Chopper techniques are employed to reduce the comparator's balance, as well as for voltage reduction. For high repeatability (in MHz), comparator delay is the limiting factor (tcomp), the tuning range of LC oscillator can be improved by incorporating dual LC oscillator instead of single band LC oscillator [5].

The required oscillator is chosen for low power and low-level disturbance: Comparing doorway coupling type and nearby transformer concentration. Consideration is given to a dual-band LC oscillator with two P-type FETs. A dual-band LC oscillator with a particular configuration in the LC tank and a self-resonating device is used. Two required cross-coupled and differential lift lashed inductors already have been reported. All of this prior research necessitated a center-tapped transformer with a high execution cost. Massive repeat generators are used to provide kHz repetition. On the RC and LC oscillator chip with 12 MHz and 30 GHz, it is suggested to reduce the aforementioned shortcomings. The schematics are shown in Figures 1 and 3. In the proposed work, CMOS LC push-push In an LC oscillator, VCO topography is utilized to enhance stage upheaval under low voltage movement. In order to avoid using various inductors, an LC tank with a PMOS push stage is used to replicate the repetition. Inductive switching method is commonly used strategy to design a switched LC VCO instead of capacitive to increase the quality factor [6]. The applicability of LC VCO is similar to oscillators used in broad-band transmission networks. Therefore, it is suggested integrating RC and LC oscillators with varying frequencies onto a single chip. This concept eliminates the need of enormous repetition generating equipment [7]. Temperature to Digital Converter (TDC) can be used in oscillator to reduce the temperature effect [8]. The proposed architecture can be used in MEMS for biomedical applications [9]. MEMS technology has been used as micro regenerators as vibrating cantilever beams which are well known as RF MEMS [10].

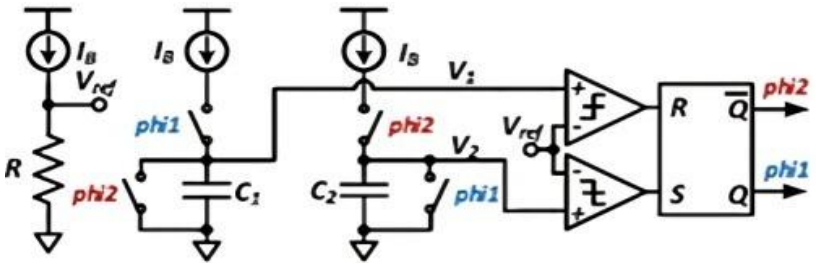


**Figure 1.** Block diagram of the RC oscillator.

## 2. Methodology

In the above circuit, there are three ammeters, one associated with a resistor and the other two associated with switches and capacitors. The two ammeters associated with switches and capacitors are directly connected to the comparator, which is used to separate the signals and produce a signal whose signal strength is high. The produced signal is connected to an SR flip-flop [7]. The RC oscillator's primary function is that of a stage shift oscillator. The circuit on the left consists of a single resistor-capacitor network whose yield voltage "drives" the data voltage by a little angle less than 90 degrees. In an unadulterated or perfect single-post RC association, it would make a stage change of no more than 90 °, and because 180 ° of stage shift is essential for influencing, at least two single-posts organizations should be used in an RC oscillator plan [11].

## 3. Reference pulse generator

Reference pulse is generated by reference voltage and comparator in the on-chip digital compensation technique. When the clock signal is high, the capacitor charges and generates a voltage Vmin connected to the positive terminal of comparator 1 ($comp_1$)

$$t_1 = R_1C + t_{comp} \tag{1}$$

Vmax is connected to the negative terminal of the comparator 2 ($comp_2$). The time $t_2$ is expressed as

$$t_2 = R_2C + t_{comp} \tag{2}$$

Pulse reference is given as

$$P_{REF} = (t_1 - t_2) \tag{3}$$

$$P_{REF} = (R_1 - R_2)\,C. \tag{4}$$

The difference between the two comparators is the reference pulse, wherein, the output of comparators is $V_1$ and $V_2$. In case of any non-ideal mismatch, the reference pulse is given as

$$Pref = (R1 - R2)\,C + .\,C.\,IB.\,(Vos1 - Vos2) + tcomp1 - tcomp2 \tag{5}$$

$V_{os1}$ and $V_{os2}$ are offset voltages of comparators. The below waveforms represent the offset voltages $V_1$ and $V_2$ and reference pulse obtained by applying the clock pulse in the proposed RC

oscillator [11]. For on-chip high precision RC and LC oscillators, the waveform obtained by the proposed relaxation oscillator is shown in Figure 2.

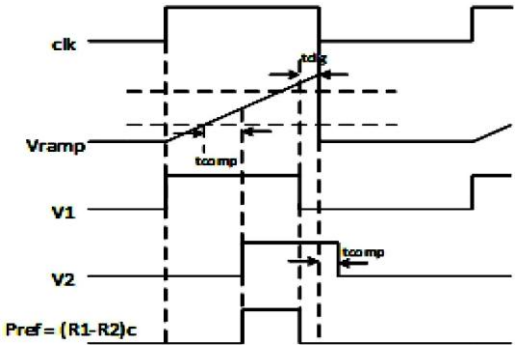


**Figure 2.** Offset voltages and reference pulse in RC oscillator.

## 4. Architecture of LC VCO

Cross-coupled LC VCO generates Ku band recurrence (12 to 18 GHz), as seen in the design above. Using a PMOS push-push frequency doubler with an inductor, Ku band frequency is converted to Ka-band frequency (26 to 40 GHz). This is carried out using 45 nm innovation and a 1.35 V supply voltage. To avoid additional inductors, a low band LC tank inductor is devised. Together, varactors and inductors form the LC tank. The differential PMOS recurrence doubler inclination current is repurposed as a bias for low band LC VCO. To compensate for the loss in the LC tank, the NMOS cross-coupled circuit is employed. The scope of the variable CV1 is modified by the $V_{cont}$. $V_{cont}$ is used to provide a variable recurrence yield. A semiconductor with an integrated source, channel, and mass is considered while creating a design for a so-called varactor. CV1 L1 is used as a balancing to avoid lengthy interconnects and undesired RF signal and DC electrical cable transmission. Due to confusion and imbalance, stage variations and adequacy balances may arise [12]. To reduce this abundance, the necessary balances and stage circuit layout are created. In the schematic, L = 0.19 nH and C = 2 pf were considered.

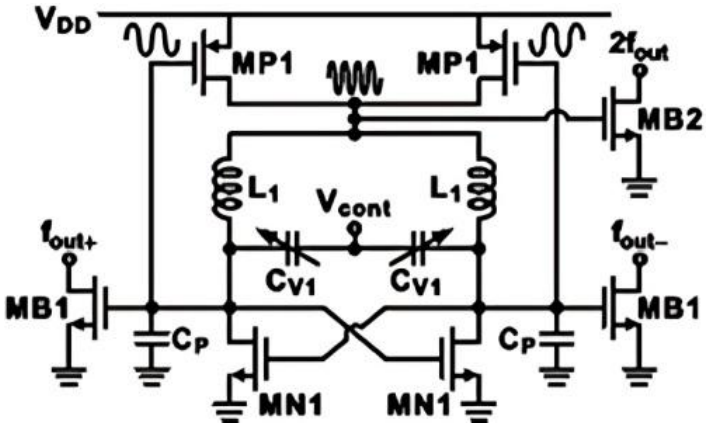


**Figure 3.** Schematic of LC VCO.

From above specifications

$$f = 8.1 \text{ GHz}.$$

By reducing the capacitance by four times, i.e., C = 2 pF, C1 = 0.5 pF, frequency is increased

$$f = 15.9 \text{ GHz}.$$

Frequency switching in 8 times

$$f = 32.67 \text{ GHz}.$$

All the MOSFETs are connected to capacitors and are controlled by a digital control that is the decoder. The inputs to the decoder are CTRL and IN. We can enhance the frequency by taking 16 steps that are reducing the capacitance by a factor of 16:

$$C = 0.5/16 = 0.03 \text{ pF [12]}$$

The above layout sub-blocks reference generator, 1 comp, 2 comp transmission gates and buffer as per the architecture of RC oscillator as shown in Figure 1 is integrated in Figure 4.

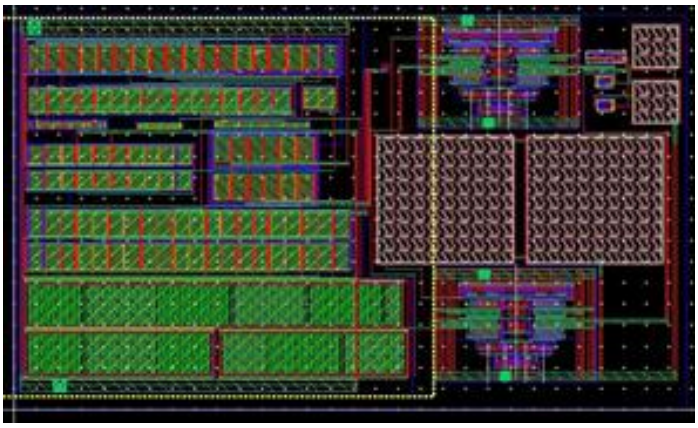

**Figure 4.** Layout of the RC oscillator.

The layout of an inductor is designed as shown below. According to the schematic in Figure 3, the inductor is designed with an L = 0.19 nH width of 11 μm.

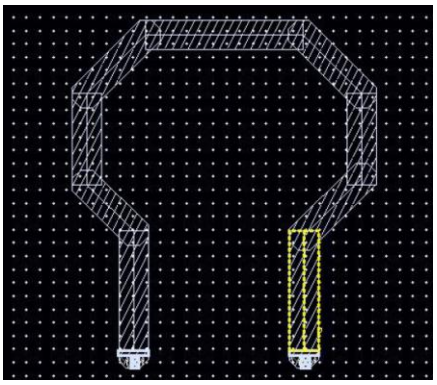

**Figure 5.** Layout of inductor.

Inductance is developed by connecting two resistors in series as shown in Figure 6.

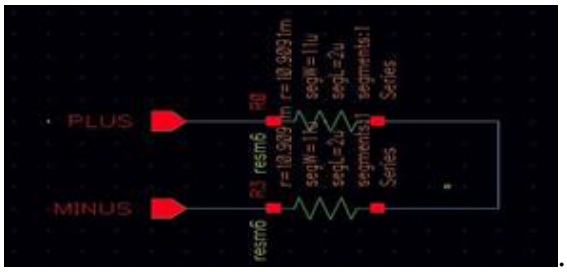


**Figure 6.** Schematic of inductor.

The layout of LC VCO is done in a symmetrical manner which is shown below. As LC VCO produces high frequency in terms of MHz, the floor plan of LC VCO is placed symmetrically [13].

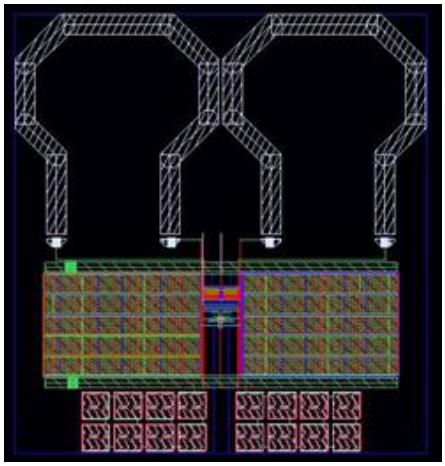

**Figure 7.** Layout of LC oscillator.

I/O cells are utilized to link the core to the outside environment. Different I/O cells are utilized for pad limited and core limited. Filler cells are used to fill the space between adjacent pads. These filler cells are used to join the pads together. Filler cells are utilized to create a connection between two pads.

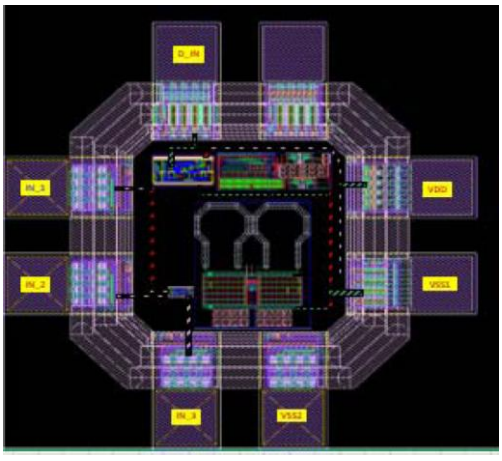

**Figure 8.** Integration of 45 nm RC and LC on single-chip.

RC and LC oscillators are placed on a single chip which is controlled by I/O cells which are shown below. The oscillator is fabricated in a 45nm process which is shown in Figure 8.

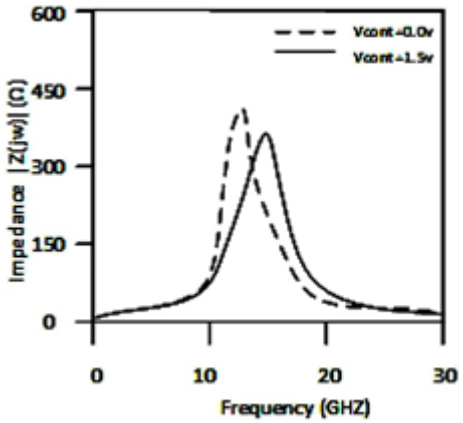


**Figure 9.** ADE simulated magnitude of resonator impedance.

Figure 9 shows the frequency versus impedance. The thick line curve is the frequency at 0 V voltage and the dotted line curve represents the frequency at 1.5 V voltage [13].

*4.1. Measurement results*

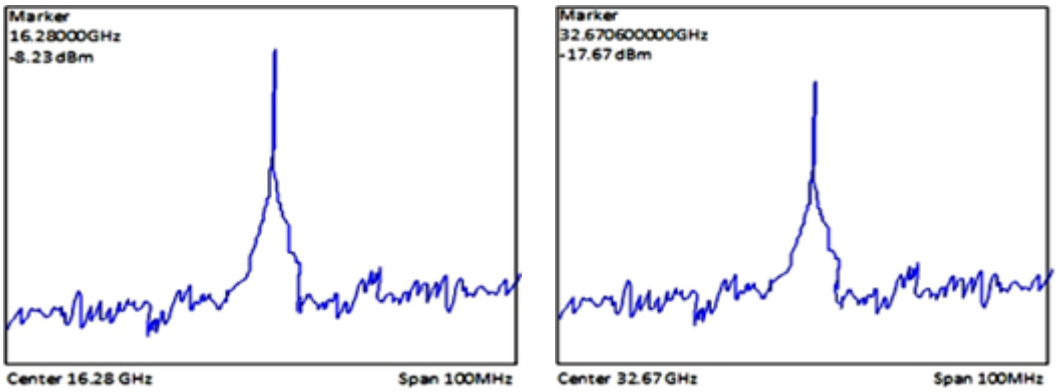


**Figure 10.** Output spectra (a) at 16.8 GHz, (b) at 32.67 GHz.

Figures 10 represents the frequencies at 16.8 GHz and 32.67 GHz, respectively. These high frequencies in terms of GHz are generated by using an LC oscillator [14].

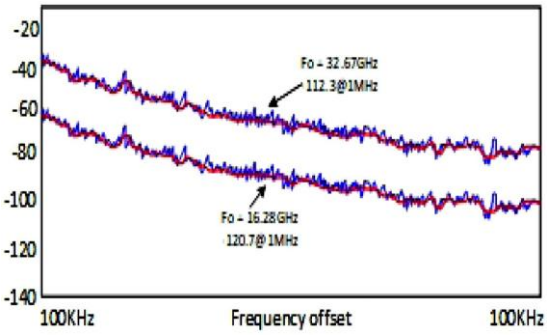


**Figure 11.** Output phase noise at 16.28 GHz and 32.67 GHz.

Figure 11 represents the frequency offset pf 112.3 at 32.67 GHz respectively. These high frequencies in terms of GHz are generated by using an LC oscillator [14].

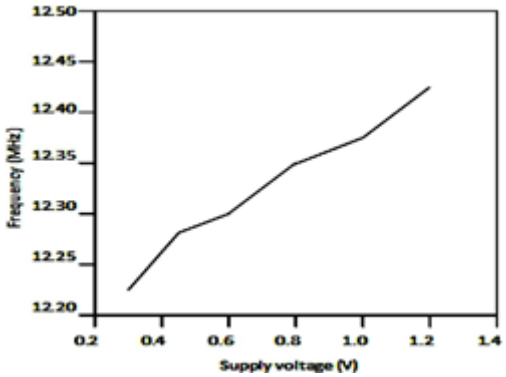


**Figure 12.** Measured output frequency versus supply voltage.

Figure 12 represents the curve for output frequency across different supply voltages, the minimum frequency at 12 MHz at 0.4 Volts and the maximum frequency at 12.4 MHz at 1.2 Volts.

Table 1 represents the comparison of RC oscillator with various frequencies at different technology nodes where the proposed work gives provides the accurate results.

**Table 1.** Frequency comparison for RC oscillator.

| Reference | Process (nm) | VDD (v) | Frequency (MHz) | Power (μw) |
|---|---|---|---|---|
| [1] | 60 | 1.2 | 0.0185 | 0.120 |
| [2] | 180 | 1.4 | 4.7 | 53 |
| [7] | 65 | 1.1 | 12.6 | 98.4 |
| [11] | 180 | 3.3 | 2 | 219.8 |
| Proposed work | 45 | 1.4 | 12 | 12.8 |

Table 2 represents the RC oscillator phase noise comparison at different technology nodes where the phase noise is positive due to its low offset at low frequencies.

**Table 2.** Phase noise comparison.

| Reference | Technology (nm) | Power (mW) | Phase noise | Supply (v) |
|---|---|---|---|---|
| [12] | 65 | 9.9 | –102.21 | 1.6 |
| [13] | 130 | 2.024 | –114.08 | 0.5 |
| [14] | 180 | 15.2 | –115 | 1.8 |
| [5] | 90 | 3 | –105.25 | 1.2 |
| Proposed work | 45 | 3 | 112.1 | 1.35 |

## 5. Conclusions

In this work, fully coordinated RC and LC VCO are implemented on a single chip on which the simulation is performed. The features of RC and LC VCO include a stable yield frequency of 12 MHz and 32 GHz, as well as a stage oscillation of 112.1@1MHz. Automated remuneration techniques are used to reduce power consumption and increase noise performance. A RC oscillator uses 12.8 W of power, but an LC oscillator uses 3 mW. This on-chip RC and LC oscillators are produced using 45 nm technologies. The frequency accuracy must be given in terms of the frequency accuracy of the reference oscillator or the frequency accuracy of the output. Typically, the parameters are represented in terms of frequency offset or frequency range from the ideal center frequency. Frequency drift is a long-lasting consequence. It was discovered that the suggested models are expertly crafted using nodes of modern technology. This on-chip oscillator is used in fully integrated system-on-chip systems that are governed by an internal voltage-controlled oscillator (VCO).

## Conflict of interest

The authors declare that there is no conflict of interest.

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