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Research article

Compact EBG structure for ground bounce noise suppression in high-speed digital systems

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Abstract: This paper proposes Inductive Enhanced-Electromagnetic Bandgap (IE-EBG) structure to suppress the Ground Bounce Noise (GBN) for high-speed digital system applications. The GBN excited between the power and ground plane pair could be a source of interference to the adjacent analog IC's on the same PCB (or) nearby devices because of radiated emission from the PCB edges. Hence, it must be suppressed at the PCB level. The proposed two-dimensional IE-EBG patterned power plane suppressed the GBN effectively over a broad frequency range. The four unit-cell IE-EBG provides a -40 dB noise suppression bandwidth of 13.567 GHz. With a substantial increment in the overall area, the nine unit-cell IE-EBG provides a -50 dB bandwidth of 19.02 GHz. The equivalent circuit modeling was developed for nine unit-cell IE-EBG and results are verified with the 3D EM simulation results. In addition, dispersion analysis was performed on the IE-EBG unit-cell to validate the lowest cut-off frequency and bandgap range. The prototype model of the proposed IE-EBG is fabricated and tested. The measured and simulated results are compared; a negligible variation is observed between them. In a multilayer PCB, the solid power plane is replaced with the 1 x 4 IE-EBG power plane and its impact on high-speed data transmission is analyzed with single-ended/differential signaling. The embedded IE-EBG with differential signaling provides optimum MEO and MEW values of 0.928 V, 0.293 ns for a random binary sequence with the 0.1 ns rise-time. Compared to single-ended signaling, embedded IE-EBG with differential signaling maintain good signal integrity and supports high-speed data transmission.

Keywords: ground bounce noise; electromagnetic bandgap structure; high-speed digital system;

signal integrity; single-ended signaling; differential signaling

1. Introduction

In recent times, there is a huge demand for high-speed electronic devices operating at high frequency, consuming low-power, and providing broad bandwidth to offer multiple wireless services to the end-users. These devices encompass multiple IC packages such as processors, memory modules, RFIC, and power supply modules are arranged close to each other over a common PCB platform. As a result of transistor switching, fast transient current will flow through narrow conducting traces present inside the IC package and between the packages on the PCB board. The rise/fall-time of the signal is as low as 0.1ns and the maximum frequency of this signal is around 10GHz. At this frequency, the conducting traces will exhibit transmission line behavior. When the transient flows through conducting traces/signal lines, a voltage drop will occur due to the inductive parasitics. The induced noise voltage will be magnified when switching multiple transistors simultaneously. It will excite cavity resonance modes within the power/ground plane pair of a PCB. The resonant modes will bounce back and forth between the power/ground plane pair and propagate outward through the substrate in all directions. It is called Ground Bounce Noise (GBN). The noise may couple to the adjacent signal traces or sensitive analog/RFIC and affects its functionality. Also, the noise may propagate through the substrate and radiate at the edges of PCB. Thus, the generated GBN will produce Signal integrity issues and Electromagnetic interference(EMI) to the nearby devices [1,2]. Hence, it is necessary to employ a suitable methodology to suppress the GBN at the PCB level.

From the literature, one of the techniques to suppress the GBN is to use a decoupling capacitor, connected between power and ground plane, as it offers a low impedance path to generated GBN. Thus, it avoids the GBN spreading throughout the whole power/ground plane [3]. This solution is bandlimited above the self-resonant frequency due to the series inductance. Embedded planar capacitors were proposed in [4]. In this approach, the major difficulties are high implementation cost and unstable characteristics of the material. To improve the bandgap/bandstop, a thin dielectric layer of high dielectric constant was inserted between the power/ground plane [5], but it increases the overall cost. Electromagnetic Bandgap structures that exhibit bandgap characteristics over a wide frequency range can be used for GBN suppression. Earlier EBG structures were extensively used for antenna applications to suppress the surface wave propagation or produce band-notch characteristics over the desired frequency spectrum. In the recent past [6–8], the signal from the antenna feedline is coupled to the adjacent EBG structures to produce band-notch characteristics at single/multiple frequency bands. In addition, the EBG structures were used to enhance the gain of single antenna element (or) arrays [9,10]. The LPC-EBG structure caused a bandgap over 4 GHz with an average suppression level of -50 dB [11]. EBG Structure using Ground Surface Perturbation Lattice [12] and Multiple Via Ground Surface Perturbation Lattices [13] were multilayer EBG structures that enhance bandgap by increasing the overall capacitive effect. A compact and wideband electromagnetic bandgap (EBG) structure with balanced slots (BS-EBG) has generated -30 dB noise isolation from 2.13 GHz–9.56 GHz [14]. L-EBG structure was proposed for -40 dB noise isolation from 510 MHz–10.35 GHz [15]. EBG optimized by the genetic algorithm was designed for wideband noise suppression from 0.01 GHz–5.6 GHz and 7.2 GHz–10.7 GHz with a suppression level of

-40 dB [16]. Glass-interposer electromagnetic bandgap structure with the defected ground plane (DGP) for suppression of power/ground noise coupling was proposed to attain -30 dB bandgap from 2.1 GHz–14.7 GHz [17]. In [18], multiring complementary split-ring resonators (CSRRs) based EBG power plane has suppressed the noise 600 MHz–13.26 GHz with an average isolation level of -40 dB. The hybrid-EBG structure was proposed for ultrawideband noise suppression from 370 MHz–20 GHz with a noise isolation level of -30 dB [19]. The non-overlapping power/ground plane was proposed to attain low IR-drop and inductance [20]. The layout used Liquid crystalline polymer substrate of thickness 100 μm with the board size of 8 cm × 5 cm with 3 × 2 power/ground plane segments produced -30 dB isolation from 1.76 GHz–9.72 GHz. In [21], nonperiodic flipped EBG was proposed to mitigate the noise over WLAN operating frequency bands such as -21 dB from 2.4 GHz–2.6 GHz and -26 dB from 5 GHz–6 GHz respectively. The spiral slot power plane has produced -40 dB noise suppression bandwidth from 0.35 GHz–20 GHz [22]. In [23], a double-square planar electromagnetic bandgap structure was proposed to obtain a -30 dB bandgap from 3.2 GHz to 21.2 GHz.

The objective of the present work is to propose an EBG structure to attain more than 18 GHz noise suppression bandwidth with an average isolation level of -50 dB. The proposed EBG was characterized both in the time- and frequency domain through numerical simulations and measurements. The effect of the proposed EBG on high-speed signal transmission was analyzed through signal integrity simulations. The proposed EBG structure was fabricated from a two-layer PCB by using a standard fabrication process, which reduces the cost of fabrication. This paper is organized as follows: The design concept of IE-EBG is discussed in section 2. The time- and frequency-domain characterization of the proposed IE-EBG is presented in section 3. Few parametric studies are performed in section 4 to enhance the noise suppression bandwidth of the IE-EBG structure. The signal integrity analysis of embedded IE-EBG with single-ended/differential signaling in a multilayer PCB is presented in section 5. Finally, the conclusions are given in section 6.

2. Design concept of proposed IE-EBG unit-cell

This section discusses the design concept of the proposed IE-EBG unit-cell. The IE-EBG unit-cell is shown in Figure 1. It is a two-layer planar PCB structure. An FR4 substrate is present between the IE-EBG power plane and the continuous ground plane. The thickness of the FR4 is 0.4 mm, dielectric constant 4.3, and a loss tangent of 0.025. The thickness of the copper layer is 0.017 mm. The physical parameters of the IE-EBG layout are shown in Table 1. The area of the IE-EBG unit-cell is 21.75 x 21.75 mm^2. In the top layer, a broad center patch is connected to the square ring through four inner bridges. The square ring is connected to the successive unit-cells through four outer bridges. The broad center patch produces a capacitive effect and the narrow inner and outer bridges produce an inductive effect. The parallel L & C generates resonance at a specific frequency band, which prohibits the EM wave propagation. The upper-frequency limit of this stopband (or) bandgap is determined by the overall inductive effect of the EBG structure. The inductive effect can be increased by increasing the length of the current path. In the proposed IE-EBG unit-cell, a narrow conducting trace is included on the four sides of the center patch and a long conducting trace in the form of a meander shape is used to connect the adjacent EBG unit-cells. Both the inner and outer conducting traces (or) bridges can enhance the inductive effect, which in turn widens the bandgap of the proposed IE-EBG unit-cell. Hence, the proposed EBG structure is

called as Inductive Enhanced-Electromagnetic Bandgap (IE-EBG) structure. In addition, the bandwidth of the stopband can be increased by including multiple numbers of IE-EBG unit-cells in the X-Y directions. The depth of the noise suppression (or) isolation can be increased by reducing the thickness of the dielectric material. The IE-EBG bandgap behavior is used to suppress the Ground Bound Noise (GBN) for high-speed digital system applications.

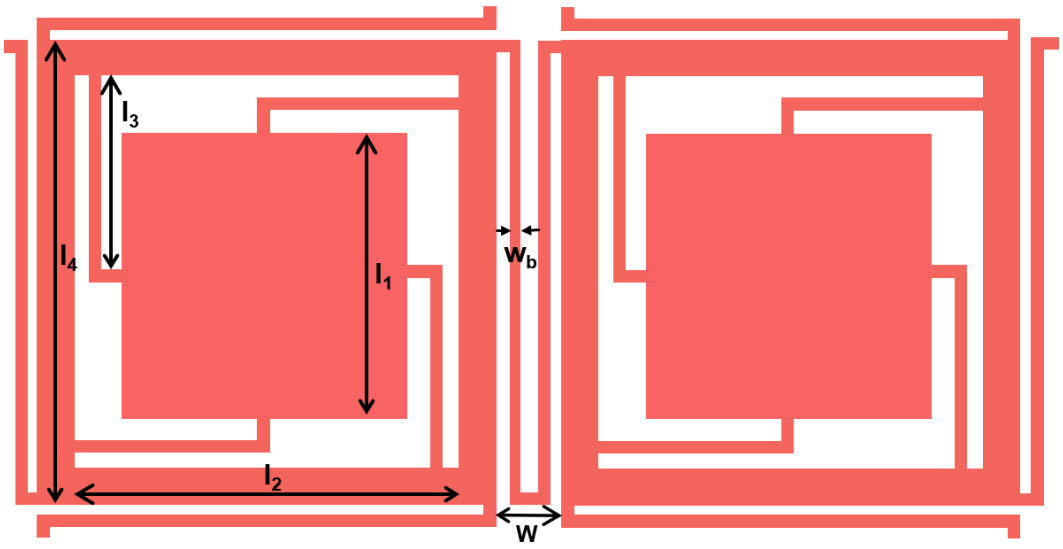

Figure 1. Top-view of two IE-EBG unit-cells with the physical parameters.

Table 1. Parameters of the IE-EBG unit-cell.

Parameters	Value (mm)	Parameters	Value (mm)
l_1	15	l_4	20.5
l_2	16.5	W	1.25
l_3	8.125	W_b	0.25

3. Characterization of proposed IE-EBG

Figure 2 shows the four unit-cell IE-EBG layout. The input is given at port-1 and the output is observed at port-2. Both the two-ports are in different IE-EBG unit-cells with reasonable spacing between them. Port-1 and port-2 are located at (10.875, 10.875), (32.625, 32.625) respectively. The area of four unit-cell IE-EBG is 43.5 x 43.5 mm^2. Port-1 represents the location of the noise source and port-2 represents the location of sensitive analog/RFICs. The noise suppression bandwidth and the associated isolation level for ports - 1 & 2 are determined through numerical simulations. CST Studio Suite, a 3D full-wave simulation software is used to characterize the proposed layout in frequency-domain and time-domain. Generally, the scattering parameter simulations are performed to determine the noise suppression bandwidth and the corresponding isolation level.

Figure 3 shows the insertion loss(S_{21}) results of a four unit-cell IE-EBG power plane and a solid power plane. The solid power and ground plane pair excite multiple cavity resonant modes. These resonant modes support the noise propagation from port-1 to port-2. But the proposed IE-EBG layout suppressed these resonant peaks and produces a broad bandgap for the noise source at port-1. The bandgap range of four unit-cell IE-EBG and solid power plane is given in Table 2. The proposed

layout provides a -40 dB noise suppression bandwidth of 13.567 GHz with peak isolation of -111.35 dB. Thus, the proposed IE-EBG layout suppressed the noise over a broad frequency range with a moderate noise suppression level.

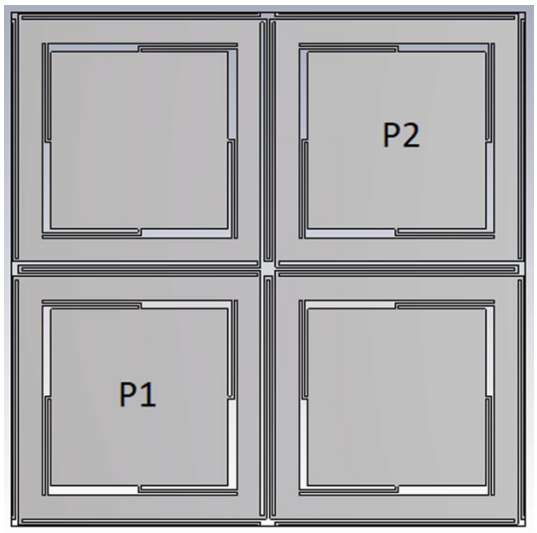

Figure 2. Four unit-cell IE-EBG layout.

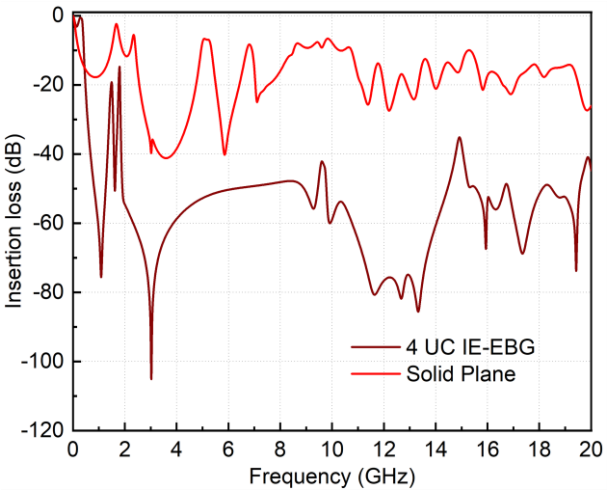

Figure 3. Insertion loss results of four unit-cell IE-EBG and solid power plane.

Table 2. Bandgap range of four unit-cell IE-EBG and solid power plane.

Layout Config.	Average Isolation level (dB)	F_{Low} (GHz)	F_{High} (GHz)	BW (GHz)	Overall BW (GHz)	Peak isolation level (dB)
Solid plane	-30	2.792	4.448	1.656	2.07	-41.18
		5.678	6.092	0.414		
4 UC IE-EBG	-40	0.670	1.330	0.66	13.567	-111.35
		1.859	14.766	12.907		

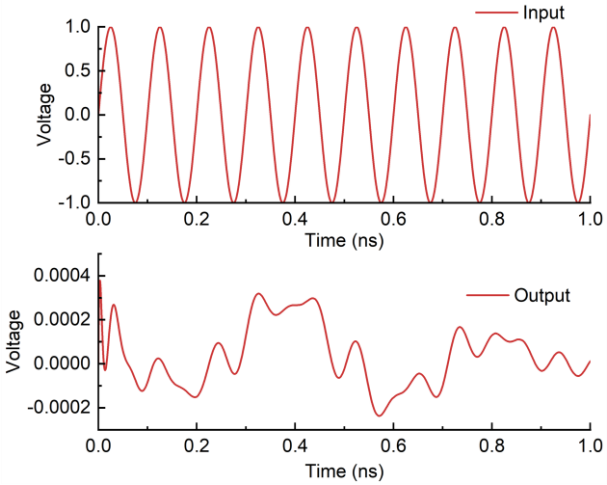

Figure 4. Sinusoidal response of four unit-cell IE-EBG.

To determine the time-domain response, a high-frequency sinusoidal waveform of 2V(p-p) is applied at port-1 and the response is observed at port-2. The time-domain input and output waveforms are shown in Figure 4. The maximum output voltage is 0.379 mV, which is 0.038% of the input voltage. Thus, the proposed four unit-cell IE-EBG suppressed the noise voltage by 99%. The next section will provide insight into the parameters that increase the bandgap of the IE-EBG power plane.

4. Parametric analysis of proposed IE-EBG layout

This section analyses the significant parameters that will affect the bandgap of the proposed IE-EBG layout. Some of the parameters to be considered are the number of unit-cells, noise source location, and the thickness of the dielectric material.

4.1. Number of unit-cell versus bandgap

The number of unit-cell is increased and the corresponding variation in the bandgap is studied in this section. The noise suppression bandwidth and the associated isolation level of four unit-cell and nine unit-cell IE-EBG are obtained through insertion loss results. Figure 5 shows the simulated insertion loss results and the parameters of interest are summarized in Table 3. From the results, the bandgap range is directly proportional to the number of unit-cells. The nine unit-cell IE-EBG provides a -50 dB noise suppression bandwidth of 18.98 GHz with peak isolation of -135.20 dB. The area of nine unit-cell IE-EBG is 65.25 x 65.25 mm^2. Compared to the four unit-cell IE-EBG, the bandwidth is increased by 40% with a substantial increment in the overall area.

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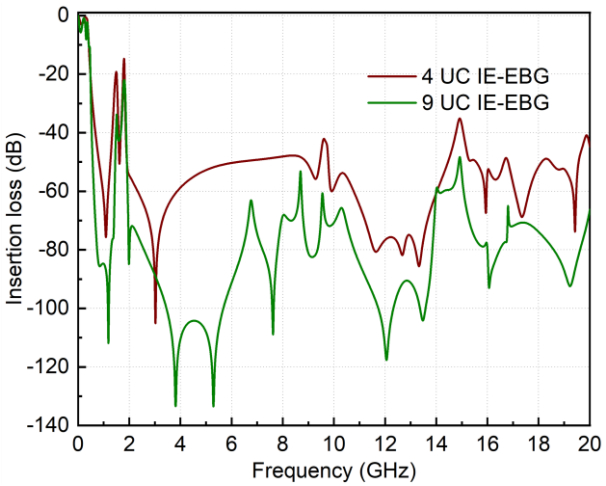


Figure 5. Insertion loss results of four and nine unit-cell IE-EBG.

Table 3. Bandgap range of four and nine unit-cell IE-EBG.

Layout config.	Average Isolation level (dB)	F_{Low} (GHz)	F_{High} (GHz)	Bandwdith (GHz)	Overall Bandwidth (GHz)
4 UC	-40	0.67	1.33	0.66	13.57
IE-EBG		1.86	14.77	12.91	
9 UC	-50	0.57	1.45	0.88	18.98
IE-EBG		1.90	20	18.1	
9 UC	-50	0.56	1.47	0.91	19.02
IE-EBG (Measured)		1.89	20	18.11	

The fabricated nine unit-cell IE-EBG is shown in Figure 6. The simulated and fabricated insertion loss results are shown in Figure 7. A marginal variation is observed between the measured and simulated results at higher frequencies due to the distributed inductive and capacitive parasitics of the IE-EBG structure.

Figure 6. Fabricated prototype of nine unit-cell IE-EBG.

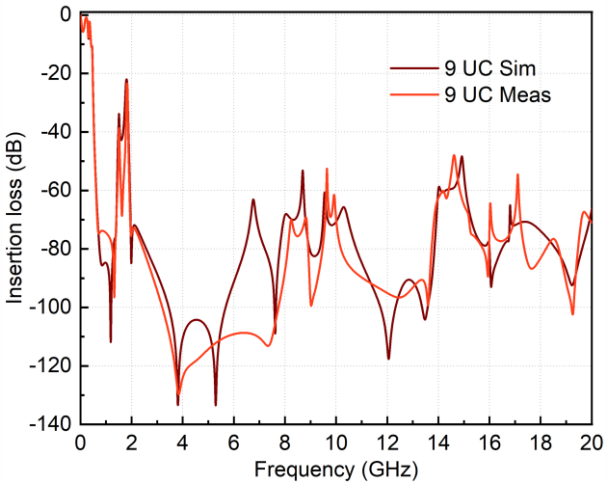


Figure 7. Measured and simulated insertion loss results of nine unit-cell IE-EBG.

4.2. Equivalent circuit modeling

The lumped equivalent circuit model of 3 x 3 IE-EBG between port-1 and port-2 is shown in Figure 8. The LC equivalent of IE-EBG unit-cell is shown inside the blue color dotted line and the LC equivalent of the outer bridge is inside the red color dotted line. The L_i, C_i represent the inductance and capacitance of the center square patch of the IE-EBG unit-cell. The L_o, C_o represent the inductance and capacitance of the square ring that is surrounded by the center patch. The tank circuit is formed by parallel L & C that exhibits filter response near the resonant frequency. The lumped parameters specified above can be expressed as [24],

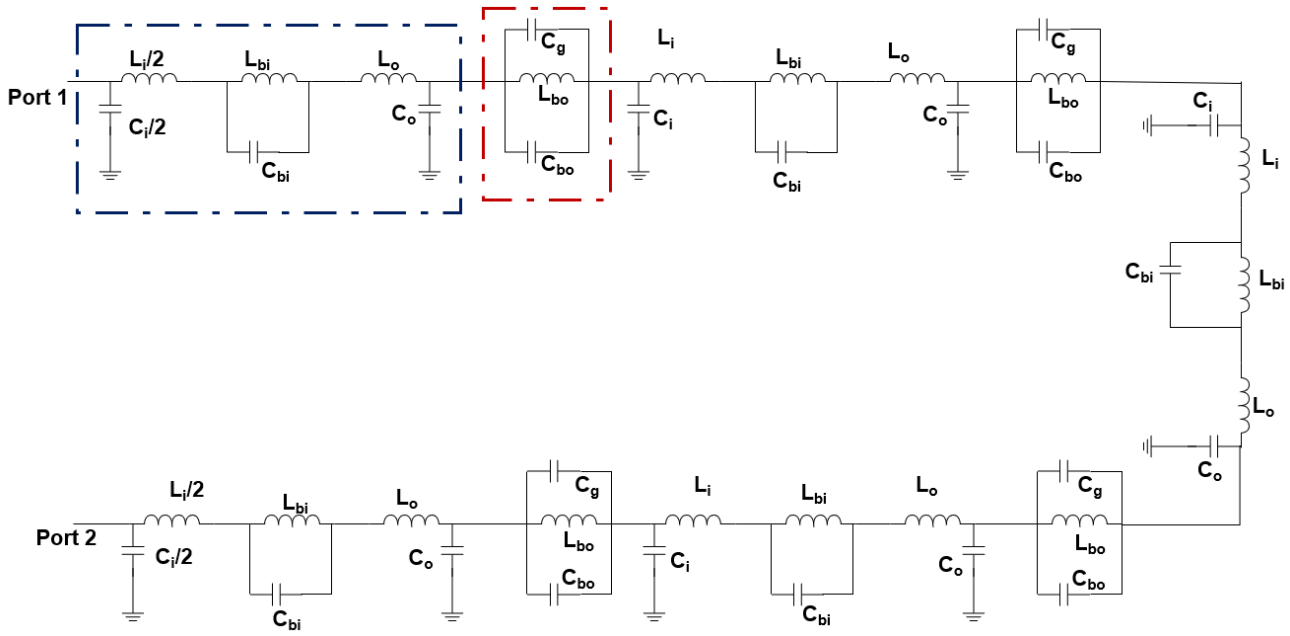


Figure 8. Equivalent circuit model of 3 x 3 IE-EBG layout.

$$L_{i=}\mu_0 d \tag{1}$$

$$C_i = \varepsilon_r \varepsilon_0 \frac{l_1^2}{d} \tag{2}$$

$$L_o = \mu_0 d \frac{2l_4}{(l_4 - l_2)} \tag{3}$$

$$C_o = \varepsilon_r \varepsilon_0 \frac{(l_4^2 - l_2^2)}{d} \tag{4}$$

where d is the thickness of the dielectric material, ε_0 and μ_0 are the permittivity and permeability of the free space. The inductance and capacitance of the inner bridge are denoted as L_{bi} and C_{bi}. It is expressed as,

$$L_{bi} = l_3.k.\ln\left(\frac{2\pi.d}{w_b}\right) \tag{5}$$

$$C_{bi} = l_3.\frac{0.67(1.41+\varepsilon_r)}{\ln\left(\frac{7.5d}{w_b}\right)} \tag{6}$$

where k = 0.2 nH/mm. The outer bridge inductance (L_{bo}) and the parallel parasitic capacitance (C_{bo}) is expressed as,

$$L_{bo} = (l_4 + w - 2w_b).k.\ln\left(\frac{2\pi d}{w_b}\right) \tag{7}$$

$$C_{bo} = (l_4 + w - 2w_b).\frac{0.67(1.41+\varepsilon_r)}{\ln\left(\frac{7.5d}{w_b}\right)} \tag{8}$$

The gap capacitance between the adjacent unit-cell is expressed as,

$$C_g = \frac{\varepsilon_0(1+\varepsilon_r)(l_4+w)}{\pi}\,\mathrm{Cosh}^{-1}\left(\frac{l_4}{w}\right) \tag{9}$$

From Equations (1)-(9), the calculated lumped parameter values are: L_i = 0.502 nH, C_i = 21.41 pF, L_o = 5.15 nH, C_o = 14.08 pF, L_{bi} = 3.75 nH, C_{bi} = 12.5 pF, L_{bo} = 9.8 nH, C_{bo} = 32.72 pF and C_g = 1.132 pF. The simulated insertion loss is shown in the Figure 9. Table 4 compares the bandgap frequency limits of the lumped model with the simulated and measured results. The calculated value is marginally deviated due to the exclusion of distributed parasitic effects in the equivalent circuit modeling process.

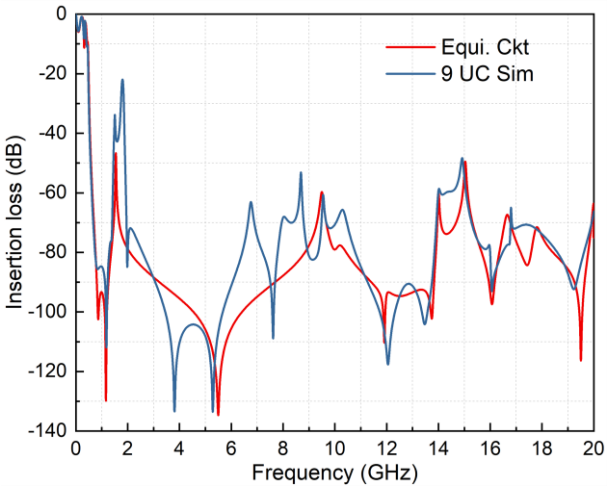


Figure 9. Insertion loss comparison between lumped model and EM simulation.

Table 4. Bandgap range comparison between lumped model, simulation and measurements.

Insertion loss results	First Bandgap (GHz)	Second Bandgap (GHZ)	Overall Bandwidth (GHz)
3D EM simulation	0.57 - 1.45	1.90 - 20	18.98
Equivalent ckt model	0.59 - 1.53	1.55 - 20	19.39
Measurements	0.56 - 1.47	1.89 - 20	19.02

The metamaterial property of the proposed EBG structure is verified by analyzing its real and imaginary values of relative permittivity. Figure 10 shows the negative permittivity in two distinct frequencies of 0.995 GHz and 2.475 GHz. The imaginary parts of the permittivity are positive. Thus, the proposed IE-EBG structure satisfies the criteria of metamaterial in these two frequencies.

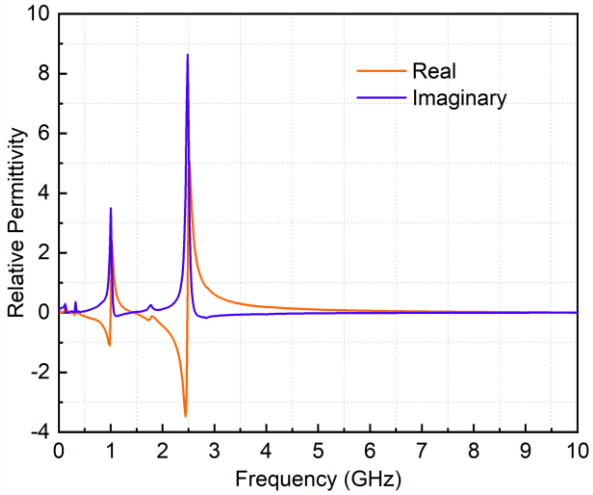


Figure 10. Relative permittivity extracted from equivalent circuit model.

4.3. Dispersion analysis of IE-EBG unit-cell

The dispersion diagram of a periodic structure represents the variation of propagation constant over the broad frequency spectrum. The important parameters of interest to be obtained from this diagram are the lowest cut-off frequency and stopband range. The Eigenmode solver of CST simulation software has been used to plot the dispersion diagram. The periodic boundary condition is applied on the X and Y-directions of the IE-EBG unit-cell. A perfect electric conductor is applied in Z_{min} and a perfect magnetic conductor in Z_{max}. An air gap of 4.8mm is applied between the top layer of IE-EBG and the PMC boundary. The simulated dispersion diagram is shown in Figure 11. From Figure 11, the lowest cut-off frequency is 0.56 GHz. In addition to the lowest cut-off frequency, the stopband behavior of the IE-EBG can be analyzed from the dispersion diagram. A narrow bandgap is present between 0.56 GHz–1.46 GHz. A wide bandgap is observed from 1.88 GHz–20 GHz except a few minor passbands around 8.7 GHz, 14.9 GHz respectively. This is consistent with the insertion loss response of the proposed 3 x 3 IE-EBG layout. The minor passband arises due to the anti-resonance caused by the parasitics of the rectangular cavity structure.

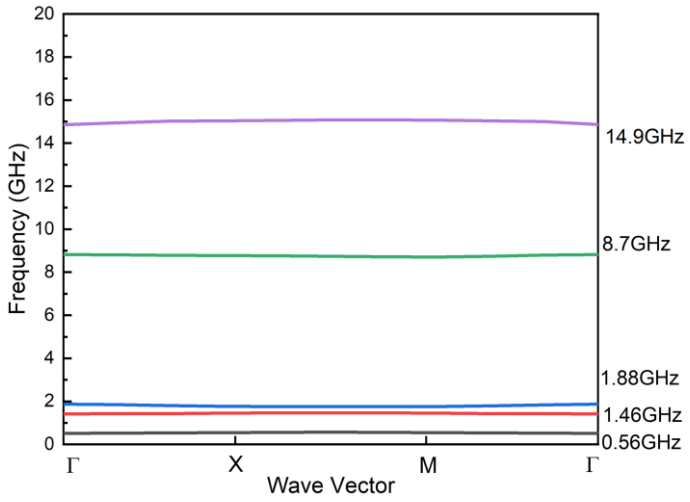


Figure 11. Dispersion diagram of IE-EBG unit-cell.

4.4. Noise source location versus bandgap

In the nine unit-cell IE-EBG layout, the noise sources are located at different unit-cells and the response of both the noise sources are observed at a common port terminal. Figure 12 shows the layout configuration for this simulation. Noise sources are located at Port-3 and 4; observation point at port-1. The simulated results are shown in Figure 13 and the parameters of interest are listed in Table 5. From the results, there is a marginal variation in the noise suppression bandwidth is observed for noise sources located at port-3 and 4. Both the two ports are at the same distance from the observation port but in different directions. It proves the Omni-direction suppression behavior of the proposed IE-EBG layout.

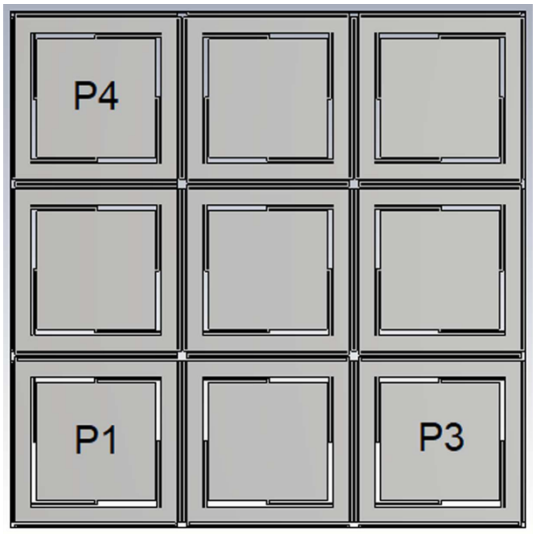


Figure 12. Noise sources at P3 and P4 of IE-EBG layout.

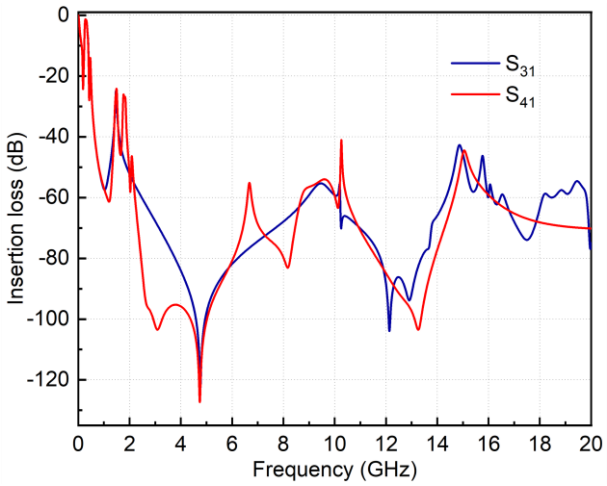


Figure 13. Insertion loss results for noise sources at P3 and P4.

Table 5. Bandgap range for noise sources at different unit-cells.

Noise source location	Average Isolation level (dB)	F_{Low} (GHz)	F_{High} (GHz)	BW (GHz)	Overall BW (GHz)
P3	-40	0.636	1.365	0.729	19.139
		1.590	20	18.41	
P4	-40	0.636	1.382	0.746	18.855
		1.891	20	18.109	

4.5. Dielectric thickness versus bandgap

In this section, the dielectric thickness of the nine unit-cell IE-EBG is varied and the corresponding noise suppression bandwidth is observed. Figure 14 shows the insertion loss results for the dielectric thickness of 0.8 mm, 0.4 mm, and 0.2 mm. The noise suppression bandwidths are listed in Table 6. The noise suppression bandwidth and the average isolation level increase while decreasing the dielectric thickness of the proposed IE-EBG layout. The IE-EBG with 0.2 mm dielectric thickness provides a maximum bandwidth of 19.807 GHz with an average isolation level of -70 dB.

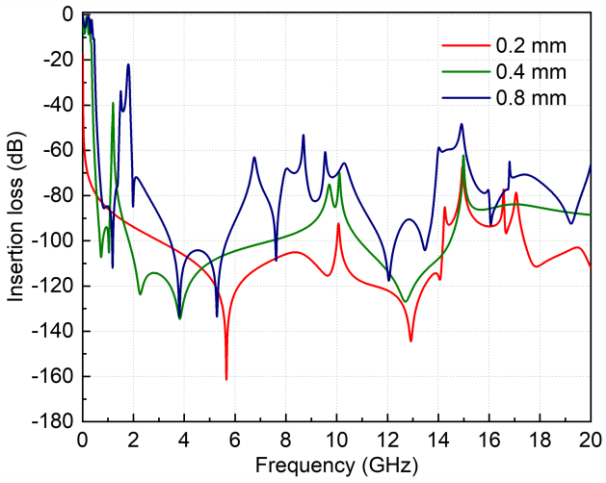


Figure 14. Insertion loss by varying FR4 thickness.

Table 6. Bandgap limits by varying FR4 thickness.

Dielectric Thickness (mm)	Average Isolation level (dB)	F_{Low} (GHz)	F_{High} (GHz)	BW (GHz)	Overall BW (GHz)
0.8	-50	0.565	1.446	0.881	18.98
		1.901	20	18.099	
0.4	-60	0.459	1.141	0.682	19.445
		1.237	20	18.763	
0.2	-70	0.193	20	19.807	19.807

From the above parametric studies, it is desirable to choose the IE-EBG layout with a fewer number of unit-cells, occupies a small area, the reasonable distance between the noise source and sensitive analog ICs and a nominal dielectric thickness to attain broad noise suppression bandwidth with a moderate isolation level.

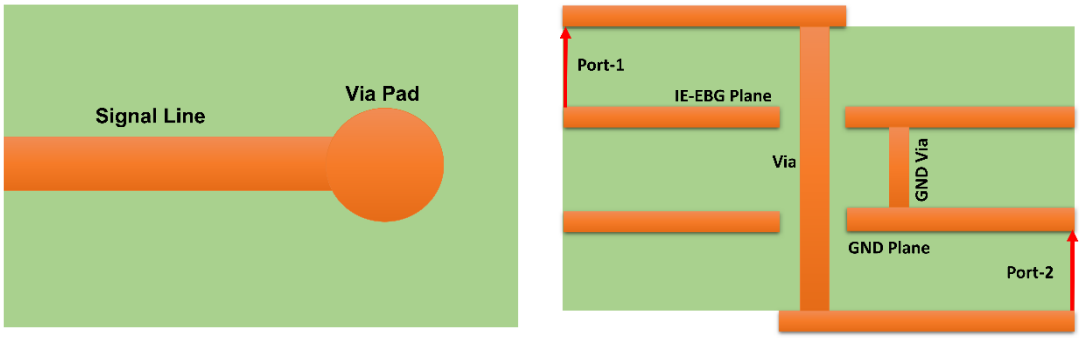
5. Signal integrity analysis of IE-EBG

5.1. IE-EBG with single-ended signaling

A 1 x 4 IE-EBG is embedded in a multilayer PCB. A transient signal with a faster edge rate is passed through the embedded IE-EBG. The impact of embedded IE-EBG on the transient signal is analyzed in this section. From Figure 15, a single-ended line on layer-1 and -4 are connected through via. The IE-EBG power plane, ground plane is in the second and third layer respectively. FR4 substrate of 0.5 mm thickness is inserted between the layers. The length and width of the single-ended line are 65.25 mm, 0.98 mm. The single-ended lines are designed to meet 50 Ω impedance. The diameter of the via, via-pad, via-clearance are 1 mm, 1.5 mm, 3.1 mm. The area of the 1 x 4 IE-EBG layer is 87 x 21.75 mm^2. The proposed embedded IE-EBG layout design in the CST studio suite software interface is shown in Figure 16.

The port-1 is applied between the top signal line to the IE-EBG power plane and port-2 is applied between the bottom signal line to the ground plane. A 2^7-1 Pseudo-Random Binary Sequence (PRBS) is launched at port-1. When the signal is passed through the via, the associated EM fields are coupled to the IE-EBG power/ground plane pair and it will excite cavity resonant modes. The cavity resonant modes are suppressed by the IE-EBG layer before it reaches the edges of PCB. As a result, the impact of radiation is reduced from the proposed IE-EBG embedded multi-layer printed circuit board.

The signal integrity at port-2 is determined through an eye diagram. The two important performance metrics of the eye diagram are Maximum Eye Open (MEO) and Maximum Eye Width(MEW). Figure 17(a) shows the simulated eye diagram for Trise = 0.1 ns and Thold = 0.2 ns. The obtained MEO and MEW values are 0.415 V, 0.198 ns. The 1 x 4 IE-EBG power plane is replaced with a solid power plane and the corresponding eye diagram is shown in Figure 17(b). The obtained MEO and MEW values are 0.926 V, 0.294 ns. For a solid power plane, the eye-pattern metrics are good for 0.1 ns rise-time due to its continuous plane profile. For embedded IE-EBG power plane, the eye-pattern metrics get worse when reducing the rise-time from 10 ns to 0.1 ns, as shown in Table 7. This is mainly due to the fact that the etched slots in the IE-EBG power plane produce impedance discontinuity to the return current. As a result, reflections will occur and it will become a dominant factor that determines the quality of eye diagram. The return path discontinuity is evidenced through Time Domain Reflectometer (TDR) as shown in Figure 18. It represents the impedance variation when the signal enters into a single-ended line from port-1. The impedance is deviated from the nominal 50 Ω impedance due to the impedance discontinuity of the IE-EBG power plane. Thus, the embedded IE-EBG has suppressed the cavity resonance but fails to support the high-speed data transmission.



(a) (b)

Figure 15. Embedded IE-EBG with single-ended signaling (a) Top view and (b) Front view.

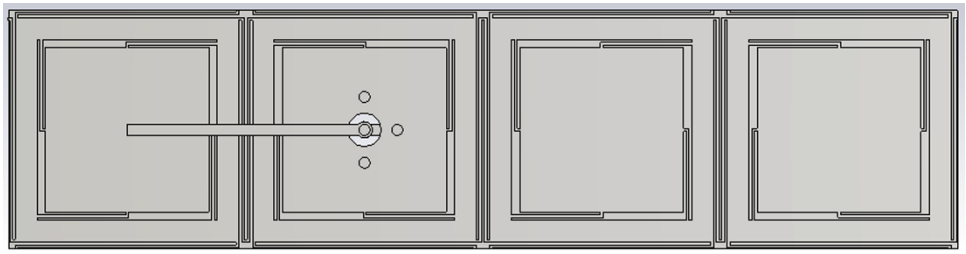
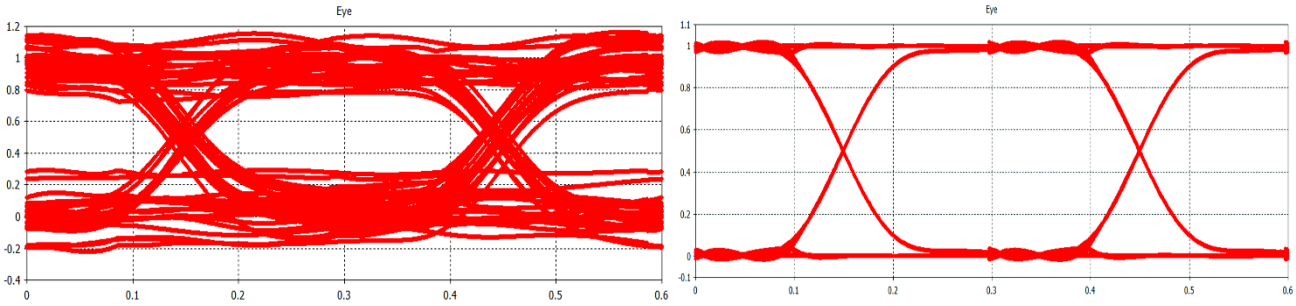


Figure 16. Embedded IE-EBG with single-ended signaling layout in simulation software interface.



(a) (b)

Figure 17. Eye-diagram for Trise = 0.1 ns and Thold = 0.2 ns (a) IE-EBG power plane (b) Solid power plane.

Table 7. Eye-diagram metrics of IE-EBG with single-ended and differential line.

Layout config.	Pulse profile (ns)		MEW (ns)		MEO (Volts)	
	Rise-time	Hold-time	Peak Value	Simulated value	Peak Value	Simulated value
Solid plane with Single-ended line	0.1	0.2	0.3	0.294	1	0.926
IE-EBG with Single-ended line	10	20	30	29.4	1	0.992
	1	2	3	2.48	1	0.492
	0.1	0.2	0.3	0.198	1	0.415
IE-EBG with Differential line	0.1	0.2	0.3	0.293	1	0.928

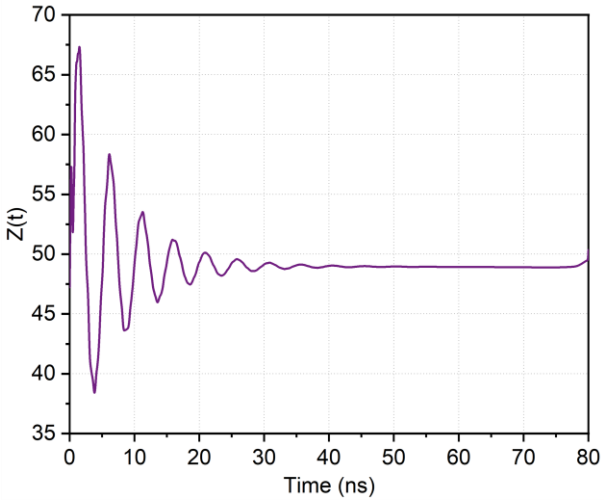
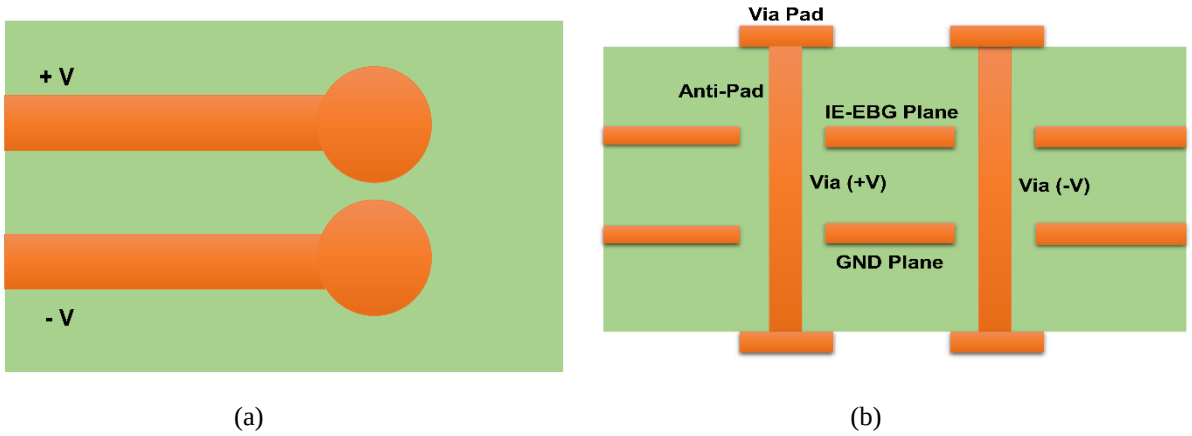


Figure 18. TDR from port-1.

5.2. IE-EBG with differential signaling

To alleviate this problem, the single-ended line must be replaced with the differential line on the top and bottom layers. Both the top and bottom differential lines are connected through differential vias. The top view and cross-sectional view of the embedded IE-EBG power plane with differential lines are shown in Figure 19. The length, width, and gap between the two lines of the differential pair are 65.25 mm, 0.36 mm, 0.12 mm respectively. The impedance of the differential line is 100 Ω. The spacing between the two via is 2.2 mm. The diameter of the via, via-pad, via-clearance are 0.36 mm, 0.6 mm, and 1.2 mm respectively. The proposed embedded IE-EBG layout with the differential line in the CST studio suite software interface is shown in Figure 20.

In differential signaling, the phase difference between the two lines is 180 degrees. The energy is kept in odd-mode when the signal is passing down the line. The EM field is tightly coupled between the two lines. The return current is passed through the adjacent line rather than the common ground. As a result, the return current will not encounter the impedance discontinuity produced by the IE-EBG power plane. The eye diagram of IE-EBG with differential signaling for 0.1 ns rise-time is shown in Figure 21. It is evident from Table 7, the eye-pattern metrics of the IE-EBG with differential signaling are marginally deviated from the peak values due to the lossy behavior of dielectrics and signal lines. Thus, the embedded IE-EBG with differential signaling maintains good differential signal integrity and supports high-speed data transmission.



(a) (b)

Figure 19. Embedded IE-EBG power plane with differential lines (a) Top view and (b) Cross-sectional view.

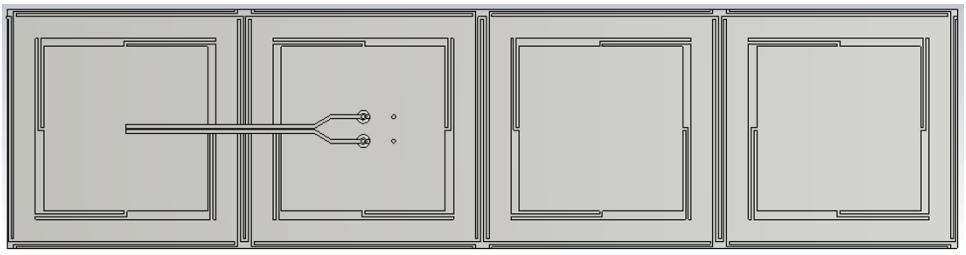


Figure 20. Embedded IE-EBG with differential signaling layout in simulation software interface.

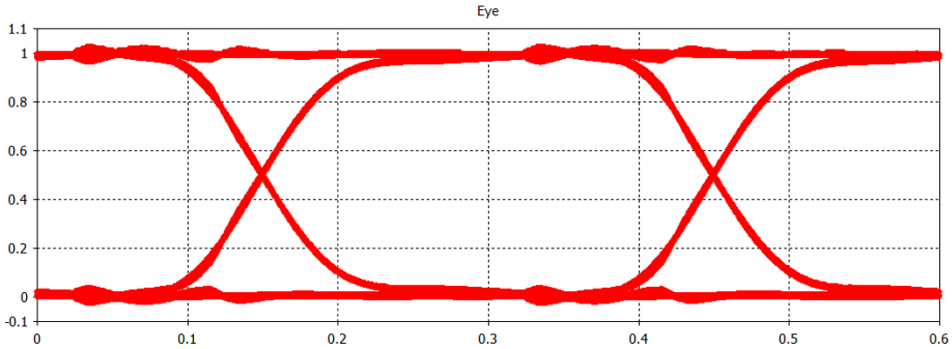


Figure 21. Eye-diagram of IE-EBG with differential signaling for Trise = 0.1 ns.

The proposed 3 x 3 IE-EBG performance metrics are compared with the existing EBG techniques from the literature in Table 8. The proposed IE-EBG provides -50 dB isolation bandwidth of 19.02 GHz, which is reasonably good in terms of high isolation level compared to existing EBG techniques for noise suppression in high-speed digital systems.

Table 8. Comparison of IE-EBG with the existing EBG structures in the literature.

Reference	EBG Technique	No. of EBG unit-cells	Noise suppression level (dB)	Bandgap range (GHz)	Overall Bandwidth (GHz)
[9]	Balanced Slot-EBG	5x2	-30	2.13 - 9.56	7.43
[10]	L-EBG	3x3	-40	0.510 - 10.35	9.84
[11]	Genetic Algorithm based EBG	10x10	-40	0.01 - 5.6 7.2 - 10.7	9.09
[12]	Glass Interposer-EBG	5x5	-30	2.1 - 14.7	12.6
[13]	Multi CSRR EBG	3x3	-40	0.6 - 13.26	12.66
[14]	Hybrid-EBG	3x3	-30	0.370 - 20	19.63
[15]	Non-overlapping power/ground plane	3x2	-30	1.76 - 9.72	7.96
[16]	Non-periodic flipped EBG	2x2	-21 -26	2.4 - 2.6 5 - 6	1.2
[17]	Spiral slot EBG	3x3	-40	0.35 - 20	19.65
[18]	Double square EBG	3x3	-30	3.2 - 21.2	18
Proposed work	IE-EBG	3x3	-50	0.56 - 1.47 1.89 - 20	19.02

6. Conclusions

The nine unit-cell IE-EBG provides a -50 dB noise suppression bandwidth of 19.02 GHz. This noise suppression level is sufficient to reduce the impact of high-frequency noise for most commercial high-speed digital system applications. The noise suppression capability is evidenced through time-domain and frequency-domain simulations. The measured results are highly correlated with the simulated results. The embedded IE-EBG with differential signaling maintains good differential signal integrity for a random binary sequence with a faster edge rate. Hence, it supports high-speed data transmission. In addition, it suppressed the high-frequency GBN noise over a broad GHz frequency range. Thus, the proposed layout can be incorporated in the modern high-speed PCBs to isolate the sensitive analog ICs from the high-frequency noise.

Conflict of interests

The Authors declare that there is no conflict of interest.

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