Electronics and Electrical Engineering

AIMS Electronics and Electrical Engineering, 6(1): 81–107.
DOI: 10.3934/electreng.2022006
Received: 10 November 2021
Revised: 26 December 2021
Accepted: 24 January 2022
Published: 10 February 2022

http://www.aimspress.com/journal/ElectrEng

Research article

Analysis of over current relay and hybrid filter including the utilization of SFCL in a distribution network with DG

Saumen Dhara[1,*], Pradip Kumar Sadhu[1] and Alok Kumar Shrivastav[2]

[1] Department of Electrical Engineering, IIT(ISM), Dhanbad, 826004, Jharkhand, India
[2] Department of Electrical Engineering, Techno International Batanagar, Kolkata, 700141, India

*** Correspondence:** Email: saumen_1978@rediffmail.com.

Abstract: Recently, as technology advances, demand for electrical energy has increased at an unprecedented rate in the power system network. With the growing importance of renewable energy assets and the global expansion of distributed generation (DG) efficiency, grid fault analysis is critical for increasing the efficiency and resilience of the power system. Apart from fault current, the interconnection of distributed generators in the distribution network results in an increase in system harmonics, as well as a halt in the operation of the overcurrent relay due to backward directed fault current. However, since the SFCL is considered to be more effective when used with distributed generators, the investigation of a protective relay due to the employment of SFCL is particularly necessary as a substitute strategy for limiting fault current in the distribution network. Additionally, many electrical customers continually require quality control, depending on the quality of the grid power it delivers and the performance of the terminal device. However, a variety of external and internal variables have an effect on the quality of energy delivered to the end consumer. It's similar to fluctuations in tension and frequency, as well as failures. Such power quality concerns erode equipment's long-term capability and performance. These concerns should be addressed in terms of harmonic reduction via the use of hybrid filtering in order to maximise the efficacy of consumer goods and overall device output. This study proposes a control strategy for the filter to eliminate harmonics and a rectification method for the overcurrent relay employing voltage components for the purpose of applying SFCL, as well as the notion of DG, in a power distribution framework. To validate the suggested approach, a malfunction with an overcurrent relay was simulated using a combination of DG and SFCL. The MATLAB/SIMULINK environment is used to simulate the desired control strategy and see the result.

Keywords: transient current limiter (TCL); pulse width modulation (PWM) inverter; boost-converter; total harmonic distortion (THD); dispersed generations (DGs); superconducting fault current limiter (SFCL); overcurrent relay; circuit breaker (CB)

1. Introduction

Nowadays, as technology advances, the need for electricity grows at an exponential pace. Additionally, customers want reliable electricity to ensure the proper functioning of products. The quality of electricity is contingent upon the voltage and frequency at which it is provided to the customer. Additionally, the majority of the load is accounted for by semiconductor-based appliances. These are non-linear devices that are mostly used for power conversion, either AC to DC or DC to AC. These semiconductor switches cause the current to be discontinuous. Additionally, it adds harmonics into the system, lowering the quality of electricity provided to the user. These power quality issues shorten the equipment's life and efficiency. Harmonics should be filtered away to improve the system's overall performance.

Additionally, with the growth of renewable energy, the various DGs in the distribution network have been extended. Subsequently, when generators with larger limitations are connected anywhere on the distribution grid, the short circuit current might increase, exceeding the limits of the existing CB operated by the protective relay. As a result, it should be used in place of circuit breakers with increased limitations to reduce the increased fault current. Thus far, it is not economically viable in light of increased costs and scientific constraint. Superconducting fault current limiters (SFCLs) have been proposed as a more effective technology for short circuit current restriction [19–23]. Generally, because to the fact that the SFCL has no resistance, it does not cause a loss when applied to a power system network. Additionally, since the activity is carried out during a quarter cycle, it enables exceptionally rapid fault current limiting [23–29]. Nonetheless, the SFCL played a critical role in defending against a malfunctioning power grid [15] network, and the reduced short circuit current caused by the use of fault current limiters in the delivery grid should also cause the relay activity to be interrupted on this front. Alternative arrangements, such as rebooting the overcurrent relay and calculating the overcurrent relay using the SFCL's voltage components, have been considered in order to mitigate the overcurrent relay's influence on SFCL [30–34]. Additionally, because interconnection of DGs in the distribution network results in opposite-direction fault current, safeguarding adjustment between the protecting relays for linking the supply grid generators' positioning, as well as the fault current limiter in the distribution grid context, is critical.

Many different filter and SFCL topologies have been proposed by researchers to address those issues that have arisen in the power distribution grid system in the past. As an example, in [1–4], the authors discuss the use of a passive filter to remove the harmonics existing in the system, although they are primarily concerned with establishing resonance with the system impedance and making the filter appropriate for filtering out harmonics present in the system. Active filters, in conjunction with control techniques, are discussed by the authors in [5] in order to enhance the system's power quality. Although active filters have some advantages over passive filters, they also have several disadvantages, including a big size, high converter ratings, and a higher cost. A control strategy based on the combination of active and passive filters is also presented here to overcome these shortcomings in order to achieve an economically viable resolution for power quality

enhancement [6]. According to the researcher in [7], the instantaneous reactive power theory is used to manage the active filter smoothly. This theory illustrates the many control algorithms and formulations of instantaneous reactive power theory that have been developed throughout time. The authors [8] discuss how to regulate a series active and a shunt passive filter by employing dual instantaneous reactive power vectorial theory. The authors [9] also provide a control technique for fault-tolerant structures in power supply, which they refer to as FTS.

In the last few years, several important research works have been imposed in the power system distribution network by researchers for various applications and benefits of SFCL, such as to validate the workability and usefulness of a novel SFCL-oriented over-current repressing method onto superconducting power electronics, an SFCL-based protecting scheme is implemented by the Authors in [35]. The benefits of resistive SFCL for quick separation of problematic sections of a multi terminal DC grid network are highlighted in [36] by utilising the quenching and recovery properties of SFCL. Several applications of SFCL in DC distribution systems are given by the authors in [37] for maintaining voltage stability, suppressing voltage fluctuations, and regulating fault current. The consistency of FEM SFCL model and appropriate method for SFCL design for the electrical energy system is suggested by the Authors in [38]. The load frequency controlling technique in a microgrid [10] and several designing and application methods of SFCL are introduced in [39] and [40] correspondingly. The research of flux coupling type SFCL for effective voltage distribution of superconducting windings during faulty conditions with the value of line impedance and the operative voltage sag frequency analysis with the optimal location of SFCL is presented on [41] and [42] respectively. Authors in [43] investigates the trigger-kind SFCL and directional overcurrent relay to limit large fault current and to prevent interrupting malfunction in accordance with the influence of SFCL. The authors of [44], [45], and [46] provide suggestions for several types of SFCL design and their most notable uses, which are detailed in the respective papers. The authors of [47] provide a method for increasing the transient stability of permanent magnetic synchronous generators (PMSGs) and lowering the capital expenditure for superconducting devices during various forms of grid disturbances by applying the Cooperative Control of SFCL. On [48], the authors describe their investigation on the impact of resistive-type SFCLs on the incremental power frequency relay of transmission lines. According to the Authors in [49], a method for protecting the power distribution system with an SFCL that makes use of voltage elements as an effective variable of the overcurrent relay is recommended, and the benefits of Flux-Coupling type of SFCL for improving the transient stability of electrical grids on the IEEE New England 39-bus test system, for the determination of systems with high pertinence, are discussed by the Authors in [50].

Essentially, the goal of this study is to manage the transient current and voltage injected by the hybrid power filter in such a manner that harmonics are minimised. For the overcurrent relay, a control strategy is proposed that allows the system to operate in both balanced and unbalanced conditions. In addition, a rectification strategy for the overcurrent relay that incorporates voltage elements and takes into account the use of SFCL with DG was projected to prevent the overcurrent relay from causing a breakdown in the power system network. The suggested secured strategy by overcurrent relay was tested using a power system simulation with DG, and the safeguard adjustment of overcurrent relays employing voltage components was studied via fault analysis in order to verify the proposed secured strategy by overcurrent relay. MATLAB SIMULINK is used to simulate and analyse the suggested control techniques. The results of the simulations are provided in this paper.

The performance analysis is carried out for different load and faults conditions with filter, SFCL and overcurrent relay. THD comparison of load voltage with and without different types of filters is

presented. The description of proposed distribution grid system with filter topology for harmonics elimination technique is discussed in section 2. Several controlling techniques for that proposed system is deliberated on section 3. Fault simulation analysis and designing of power distribution network modelling with trigger-type SFCL is discussed in section 4. The section 5 represents the subsequent Simulation Results and Discussion. Section 6 represents the proposed overcurrent relays functional flow diagram and comparison of various schemes. The sensitivity analysis is depicted on section 7 and finally section 8 gives the brief conclusion and future scope of the work.

2. Design of series active filter

The three-phase Voltage Source Inverter (VSI) [8] is used to implement the series active filter that is used for power quality enhancement. The source impedance is coupled to the voltage source impedance (VSI) using an ideal 1:1 transformer, as illustrated in Figure 1. A series of capacitors is connected at the input of the VSI in order to generate a steady output voltage. When the passive filter is linked at the point of common coupling, it is possible to remove higher-order harmonics (PCC). In addition to VSI, a ripple filter is connected in series with it. The characteristics of the filters are developed in accordance with the loading criteria of the transformer. The hybrid power filter adjusts for distortion and unbalanced voltages as a result of the PI current regulator and synchronised 6-pulse generator-based control method used by the PI current regulator. In addition, the harmonics that occur in the neutral wire are decreased as a result of the use of series APF [13].

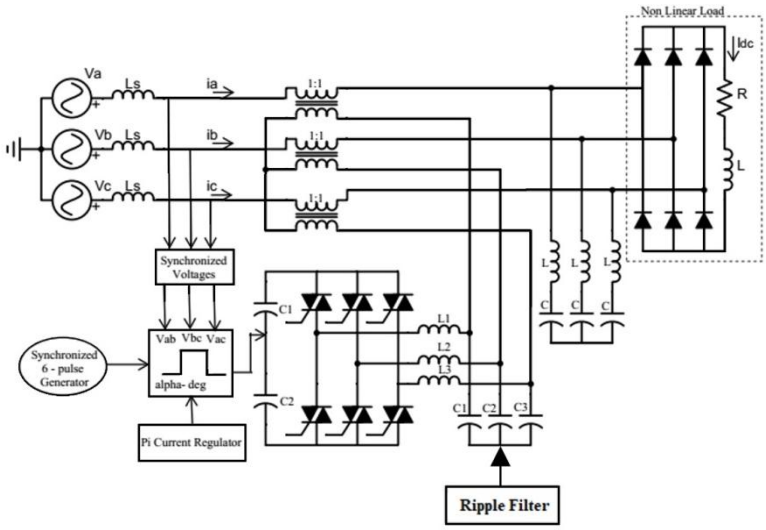


Figure 1. Three-phase VSI control block diagram.

2.1. State equation of series active filter

Despite this, modelling of a series active filter is used to manage the performance of the filter. In accordance with Figure 2, the model is carried out in a 2-dimensional ($\alpha - \beta$ dimensional) stationary reference frame. As a result, using Clarke's transformation [11,12],

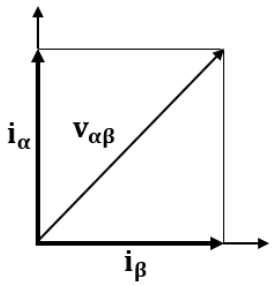


Figure 2. Voltage vector diagram in a $\alpha - \beta$ reference frame.

the system voltage and current is represented as:

$$v = [v_a \quad v_b]^T \tag{1}$$

$$i = [i_a \;\; i_b \;\; i_c \;\;]^T \tag{2}$$

The instantaneous value of real power is calculated in the stationary reference frame $0 - \alpha - \beta$.

$$p_{3\Phi}(t) = v_\alpha i_\alpha + v_\beta i_\beta + v_0 i_0 \tag{3}$$

$$p_{3\varphi}(t) = p + p_0 \tag{4}$$

The zero-sequence power p_0 is the product of zero-sequence voltage v_0 and zero-sequence current i_0 respectively. The instantaneous real power can be expressed as:

$$p = v_\alpha i_\alpha + v_\beta i_\beta \tag{5}$$

The power in vectorial form using dot product can be expressed as:

$$p = i_{\alpha\beta}^T v_{\alpha\beta} \tag{6}$$

Hence the α-β coordinates are represented the transposed current vector $i_{\alpha\beta}^T$ and voltage vector $v_{\alpha\beta}$ by the Eqs (7) and (8) respectively.

$$i_{\alpha\beta} = [i_\alpha i_\beta]^T \tag{7}$$

$$v_{\alpha\beta} = [v_\alpha v_\beta]^T \tag{8}$$

The instantaneous imaginary power can be expressed as:

$$q = v_\alpha i_\beta - v_\beta i_\alpha \tag{9}$$

Also, in vector form expressed as:

$$q = i_{\alpha\beta\perp}^T v_{\alpha\beta} \tag{10}$$

The transposed of current vector $i_{\alpha\beta\perp}^T$ is perpendicular to $i_{\alpha\beta}$ and shown in Eq (11) as:

$$i_{\alpha\beta\perp} = [i_\beta - i_\beta]^T \tag{11}$$

Thus, the instantaneous real and reactive power in matrix form can be expressed as:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} i_{\alpha\beta}^T \\ i_{\alpha\beta\perp}^T \end{bmatrix} v_{\alpha\beta} \tag{12}$$

Therefore, the voltage vector equation will be:

$$v_{\alpha\beta} = \frac{p}{i_{\alpha\beta}^2} i_{\alpha\beta} + \frac{q}{i_{\alpha\beta}^2} i_{\alpha\beta\perp} \tag{13}$$

2.2. Control strategy

The control technique, which is based on the theory of instantaneous reactive power [14], is intended to reduce harmonics and give high-quality power to the end user. To accomplish this situation, a three-phase VSI controller injects a regulated reference voltage as illustrated in Figure 1. The controller's gate pulse is regulated by a PI controller. The flow diagram in Figure 3 illustrates the rationale of the control approach.

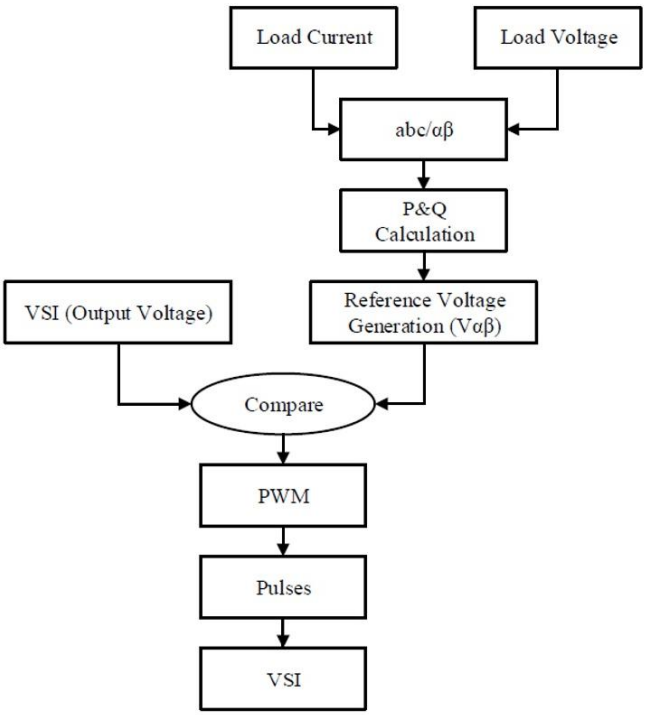


Figure 3. Control technique flow diagram.

The voltage under linear, resistive and balance load can be expressed as:

$$v = R_e i \tag{14}$$

Thus, the average power received by the load is given by:

$$p_l = i^2 R_e \tag{15}$$

$$V_{pcc\alpha\beta} = R_e i_{\alpha\beta} \tag{16}$$

$$v_{pcc\alpha\beta} = \frac{p_L}{I_1^2} i_{\alpha\beta} \tag{17}$$

Therefore, the load voltage can be written as:

$$v_{L\alpha\beta} = \frac{p_L}{i_{\alpha\beta}^2} i_{\alpha\beta} + \frac{q_L}{i_{\alpha\beta}^2} i_{\alpha\beta\perp} \tag{18}$$

The compensating voltage of the controller can be expressed as:

$$v_{c\alpha\beta}^* = v_{pcc\alpha\beta} - v_{L\alpha\beta} \tag{19}$$

Thus, the compensating voltage obtained from Eqs (18) and (19) can be modified as:

$$v_{c\alpha\beta}^* = \left(\frac{p_L}{i_1^2} - \frac{q_L}{i_{\alpha\beta}^2}\right) i_{\alpha\beta} - \frac{q_L}{i_{\alpha\beta}^2} i_{\alpha\beta\perp} \tag{20}$$

2.3. Design of PI controller

The controller's switching function is developed using the PI controller. The reference voltage is represented in Eq (20) and the PI controller block design is shown in Figure 4.

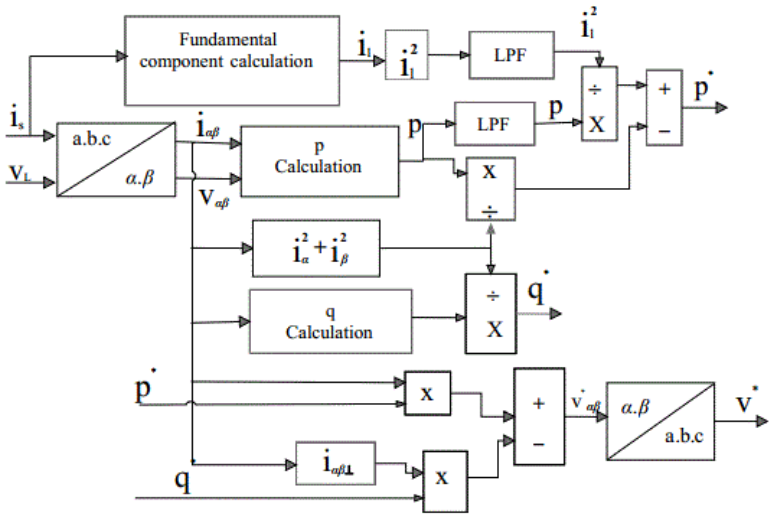


Figure 4. PI controller block diagram.

The current is proportional to the reference value of the controller's output voltage. A PI controller is utilised to cause the error. The real value is close to the reference value, and the controller gain values are computed to minimise error. If this condition is met optimally, the serial controller linked to the source inductance enhances the load's energy efficiency and filters harmonics using a hybrid filter, hence increasing the system's output [51].

3. Fault simulation analysis

3.1. Designing of power distribution network

To assess the suggested modification technique's suitability, short circuit tests were conducted and occurrences of overcurrent relay malfunction in a distribution network connected with DG were explored. Figure 5 depicts the diagrammatic depiction of the distribution network linked with DG. The primary distribution network is constructed using the primary supply with double feeder lines linked to the secondary portion of the primary transformer. A 7 MW load is linked at a position 7 kilometres and 20 kilometres from the bus, and the top feeder line is 20 kilometres long. The superconducting fault current limiter [17,18] is installed on the top feeder conductor's entry, and the impedance Z = 4.73 + j8.39 [percentage Ω/km] is adjusted for each feeder line. A 0.7 MW load is connected at seven and 25 kilometres from the bus, respectively, and the whole length of the bottom feeder line is 27 kilometres.

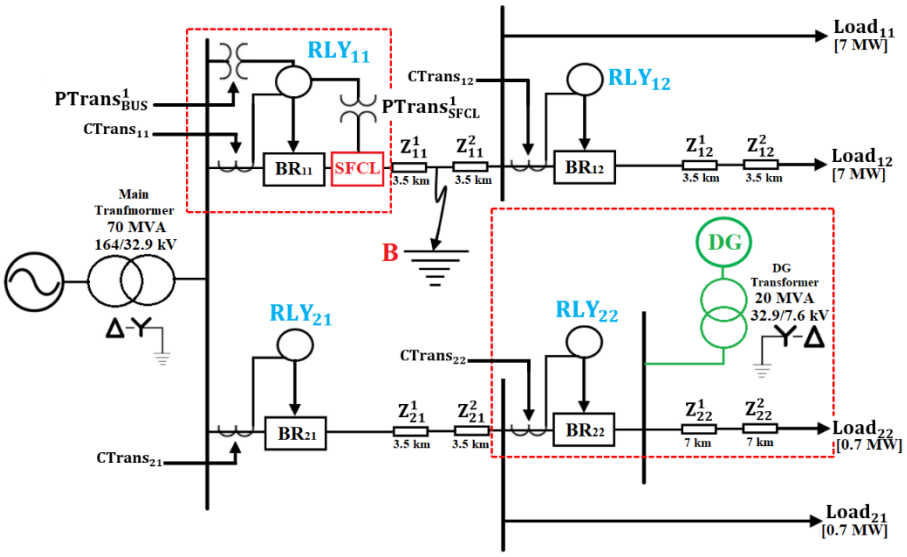


Figure 5. Schematic diagram for safety management analysis of overcurrent relays utilizing voltage elements for the implementation of superconducting fault current limiter in a power distribution grid with the distributed generator.

The L-L-L-G fault was calculated at the 3.5 km point distance from the top feeder conductor for simulation of overcurrent relay dysfunction and the distributed generator was coupled on 7 km point distance from the bottom feeder conductor. The overcurrent relay of the top feeder line (RLY_{11}) can be anticipated to have functioned, in this present condition. Nonetheless, because of the impact of the DG of the bottom feeder line, the overcurrent relay of the bottom feeder line (RLY_{22}) near to the DG is predicted to be tripped ahead of the activity of (RLY_{11}).

3.2. Analysis of OCR's working features

The current overcurrent relay, which is installed at the location of the circuit breaker installation, estimates the current flowing through the current transformer. The estimated values of currents are

turned into symmetrical elements, and a positive element between the symmetrical elements is used to conduct the computation in order to complete the calculation. Typically, the overcurrent relay's working features equations are described by the Eqs (21) and (22) and the tripping time (T_{r1}) of the overcurrent relay has the inverse property of the overcurrent relay's working features equations.

$$T_{r1} = TS.\left(\frac{G}{N^{l}-1} + H\right) \tag{21}$$

$$N = \frac{A_f}{A_{Peak}} \tag{22}$$

Where TS denotes a time span, N denotes an activity pointer value and G, H, l are the constants. Moreover, A_f designates the peak value of current throughout the CT and A_{Peak} is the peak value of current in view of line limits and load adjustment.

Also, SFCL creates tripping time deferral of the overcurrent relay during functioning. So, the rectification process by seeing the activity of the SFCL is essential. The proposed rectification technique incorporates the voltage of SFCL (E_{SFCL}) and the potential of bus (E_{BUS}) elements in the working pointer grade as represented in Eq (23).

$$N' = \frac{C_1 E_{Peak}}{E_{BUS} - C_2 E_{SFCL}}\left(\frac{A_f}{A_{Peak}}\right) \tag{23}$$

While no SFCL is introduced into the system, the peak value of the voltage (A_{Peak}) is changed to the correct range, and the working pointer grade may be set to be comparable to the working pointer one (N) of (22) by employing the rectification method (N') in the overcurrent relay. For example, when the standard procedure by employing (22) is implemented in the presence of SFCL, the values of (N) drop, A_f lowers, and T_{r1} increases, deferring tripping time. In the functioning pointer grade of the overcurrent relay, the rectification procedure described in (23) is used. Nevertheless, the numerator of Eq (23) contributes to the compensation for reduced fault current A_f during SFCL operation by subtracting the potential created in the superconducting fault current limiter (E_{SFCL}) from the reduced bus potential (E_{BUS}). In (23), the rectification constant C_2 may be altered to a variety of standard values depending on the kind of fault [52], and the rectification constant C_1 is adjusted to be comparable to the overcurrent relay setting value if the system does not include an SFCL. With the suggested rectification technique employing the activity pointer value of (23), the working duration of the overcurrent relay is enumerated and the effect of the fault current limiter is reduced while the fault current is decreased by the fault current limiter's activity. Table 1 summarises the chosen values for several parameters.

Hence, C_1 and C_2 are the constants of rectification, E_{SFCL} and E_{BUS} denote the SFCL voltage and bus voltage calculated from the individual potential transformer (PT). Figure 6 showed the overcurrent relays' operating characteristic curves for each instance, where N denotes the activity pointer value specified by Eqs (22) and (23). The overcurrent relay's tripping interval is represented by T_{r1}. $SFCL^{(Ex)}$ denotes that it is not linked to the system, but $SFCL^{(In)}$ indicates that it is connected. Figure 6(a) depicts the functioning feature graphical answers for the overcurrent relays when no DG is connected. As seen in Figure 6(a), when the fault occurs at position B of Figure 5, RLY_{11} operates independently.

Table 1. Variables of overcurrent relay.

Particulars	Index	Data	Unit
RLY_{11}	TS	0.5	-
	G	41.85	-
	H	2.084	-
	l	2.95	-
	A_{Peak}	0.5	[kA]
	E_{Peak}	14.96	[kV]
	C_1	0.85	-
	C_2	2	
RLY_{22}	TS	0.28	-
	G	41.85	-
	H	2.084	-
	l	2.95	-
	A_{Peak}	0.10	[kA]

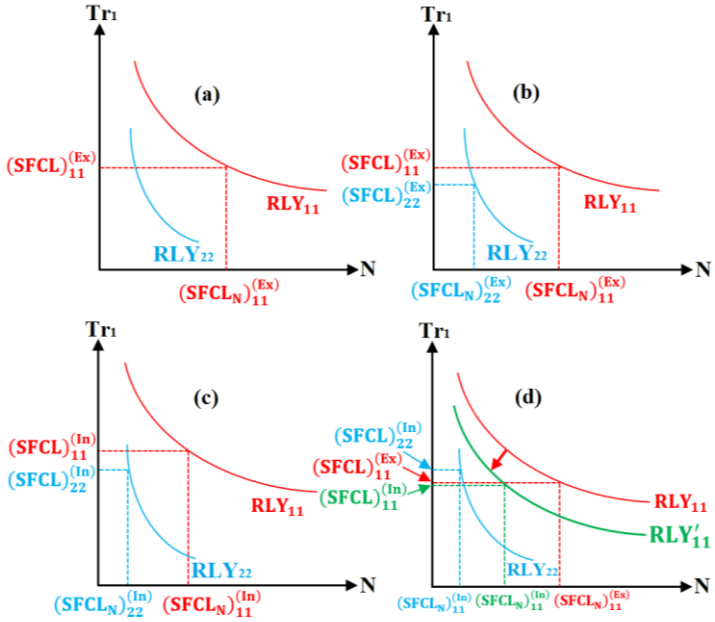


Figure 6. Working feature graphical responses of the overcurrent relays due to activity pointer value for every instance. (a) applying present overcurrent relays ($RLY11$, $RLY22$) in the distribution grid besides distributed generator. (b) applying present overcurrent relays ($RLY11$, $RLY22$) in the distribution grid including distributed generator. (c) applying present overcurrent relays ($RLY11$, $RLY22$) in the distribution grid combined with distributed generator and superconducting fault current limiter. (d) applying overcurrent relay with proposed rectification process ($RLY11$) and present overcurrent relay ($RLY22$) in the distribution grid combined with distributed generator and superconducting fault current limiter.

Figure 6(b) represented the situation wherever distributed generator is associated in the power distribution network similar to Figure 6(a). In that event the distributed generator is associated, so the performance for the short circuit current to the distributed generator additionally happens, whose effect makes the RLY_{22} to active, i.e., dysfunction. For the instance, if the RLY_{22} is adjusting into the small adjusting value, the RLY_{22} could be worked however the short circuit current from the DG is low. Due to the opposite fault current, the activity of the RLY_{22} from DG can be repressed, as the past avoidance of the overcurrent relay's dysfunction, the directional overcurrent relay is useful in place of RLY_{22}.

The utility of SFCL in the distribution grid is represented by Figure 6(c). The sensed short circuit current by the RLY_{11} and RLY_{22} is decreased by the SFCL. Thus, the tripping time of the RLY_{11} was deferred into $(SFCL)_{11}^{(In)}$ from $(SFCL)_{11}^{(Ex)}$, as demonstrated in Figure 6(b). Also, the tripping duration of the RLY_{22} was additionally deferred into $(SFCL)_{22}^{(In)}$ from $(SFCL)_{22}^{(Ex)}$ as demonstrated in Figure 6(b). Nonetheless, the RLY_{22} until works specifically at $(SFCL)_{22}^{(In)}$ earlier the activity of the $R_{11}(SFCL)_{11}^{(In)}$, causes a needless disturbing activity.

Similar to Figure 6(c), Figure 6(d) signifies the condition that the recommended rectification technique in the RLY_{11} is useful for a similar network. The working feature graphical response of the RLY_{11} by utilizing the proposed rectification technique is driven into $RLY_{11}^{'}$ from RLY_{11} as shown with a solid green shading curve in Figure 6(d). Since, the proposed rectification procedure for RLY_{22} isn't implemented, as SFCL isn't introduced in the feeder of RLY_{22}. The RLY_{11} can be acclimated to be functioned earlier the activity of the RLY_{22} exclude the variety of the working interval as shown with $(SFCL)_{11}^{(In)}$ and $(SFCL)_{11}^{(Ex)}$ in Figure 6(d) by implementing the recommended rectification technique into the RLY_{11}.

3.3. Design of trigger-kind superconducting fault current limiter

The SFCL is an active safety apparatus to restrict short circuit current. From viewpoint of the benefits of SFCL, usually, its resistance is zero so it has loss-free and during the fault, its rapid and efficient activity helps to restrict the fault current instantly. For research purposes, various kinds of SFCL have been considered, for example, trigger-kind, flux-lock-kind, resistance-kind, transformer-kind, and hybrid kind SFCLs [25–29].

Among the several types of SFCL used in Korea's power grid network, the trigger type fault current limiter circuit is largely used by the Korean Power Industry, which is consistently leading the study to demonstrate the usefulness of trigger-type superconducting fault current limiters [16]. Additionally, because the trigger-type SFCL is efficient at shrinking the size of the high-temperature superconductor in order to avoid a short circuit current generated by the current limiting reactor, and also because it is economical, it can help reduce the cost of high-temperature superconductor, it has garnered attention in the power industry [53]. The parameter values in Table 2 are itemised, and the layout figure for the trigger-kind SFCL is applied on the simulated distribution grid as shown in Figure 7 and Figure 8 correspondingly.

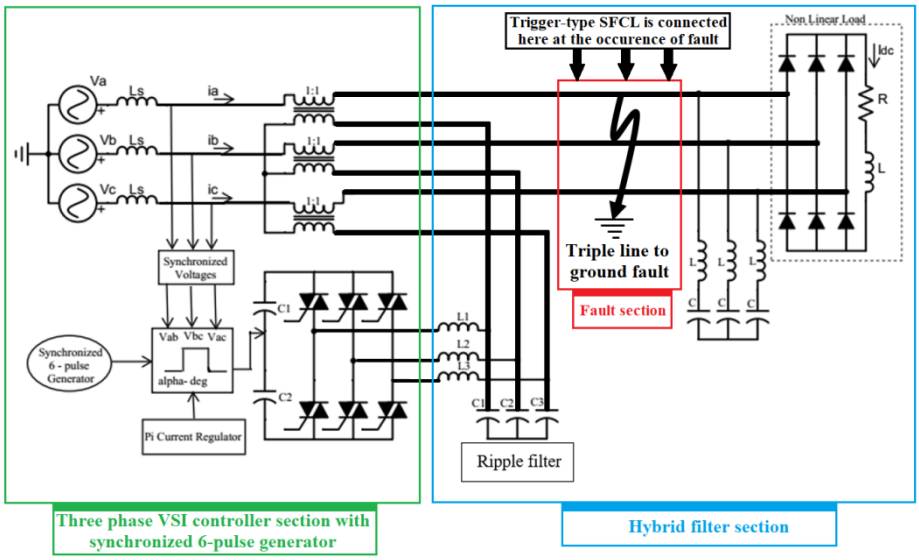


Figure 7. Occurrence of triple line to ground fault between VSI control and hybrid filter section and according to Figure 8. Trigger SFCL is placed on that indicated position.

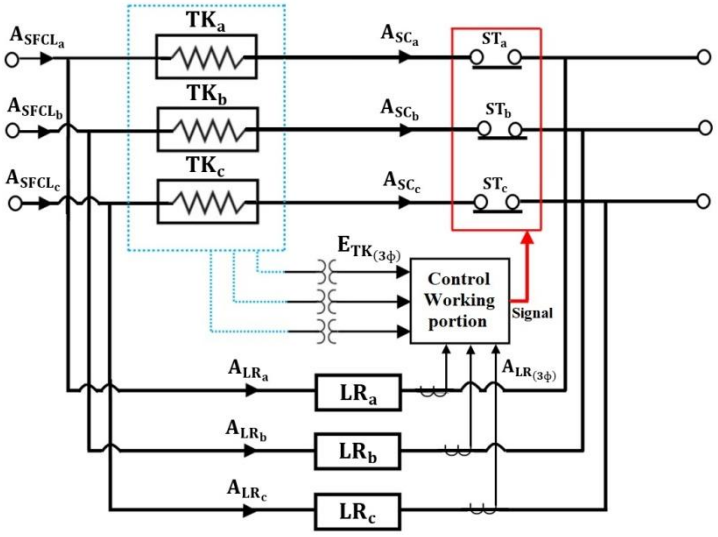


Figure 8. Trigger-kind SFCL layout drawing.

Table 2. Trigger-kind SFCL variables.

Particulars	Index	Data	Unit
HTSCs$\begin{pmatrix} TK_a, TK_b \ and \\ TK_c \end{pmatrix}$ & CLRs$\begin{pmatrix} LR_a, LR_b \ and \\ LR_c \end{pmatrix}$	Converging resistance ($R_n^{'}$) Critical current (A_c) Current limiting reactor	5 4.5 J0.9	[Ω] [kA] [Ω]
SWs $\begin{pmatrix} ST_a, ST_b \ and \\ ST_c \end{pmatrix}$	E_{set} A_{Reset}	3 0.7	[kV] [kA]

4. Fault simulation analysis

In a MATLAB/SIMULINK system, the simulation results are obtained for both balanced and unbalanced load scenarios as shown in Figure 1. Tables 3 and 4 provide the simulation and filter settings. The simulation is run with increasing load impedance and varied load values, using the actual device specifications.

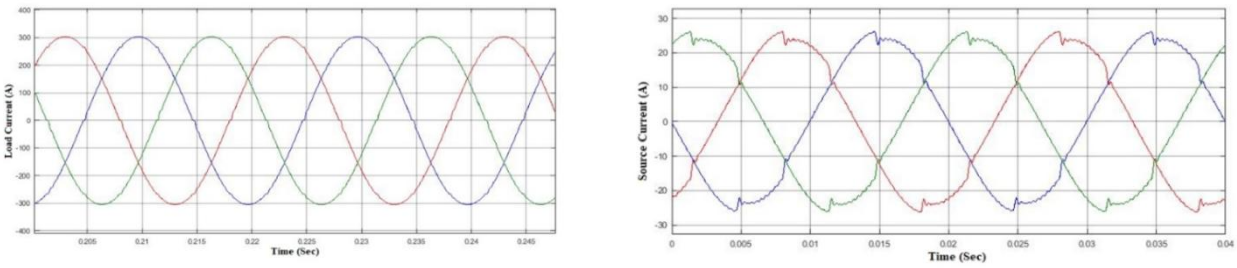
Table 3. Simulink model (System parameters) specifications.

Sl. No.	Particulars	Value
1	Voltage	200 V
2	Switching frequency	10 kHz
3	Resistance	4.5 Ω
4	Inductance	4.6 mH
5	Transformer turns ratio	1:1

Table 4. Filter parameter specifications.

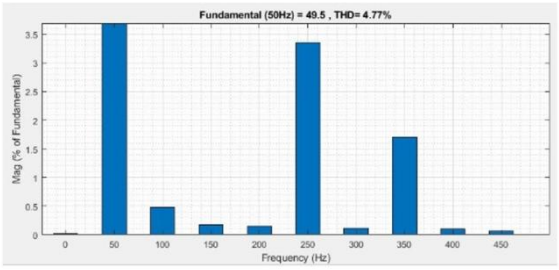
Sl. No.	Filter Parameter	Value
1	L_5	13.5 mH
2	C_5	30 μF
3	L_7	6.75 mH
4	C_7	30 μF
5	L_r	13.5 mH
6	C_r	50 μF
7	R_L	25 Ω
8	L_L	55 mH
9	C_L	2200 μF

Figures 9(a) and 9(b) depict the load current and source current of phase A in the absence of a controller. Figure 9(c) illustrates the total harmonic distortion (THD) of load current, which exceeds IEEE norms. To remove the system's harmonics, a single passive filter is connected in the circuit, as seen in Figure 9(d) and 9(e). The source and load current waveforms are displayed in Figure 9(d) and 9(e) respectively. Figure 9(f) illustrates the THD of the load current.

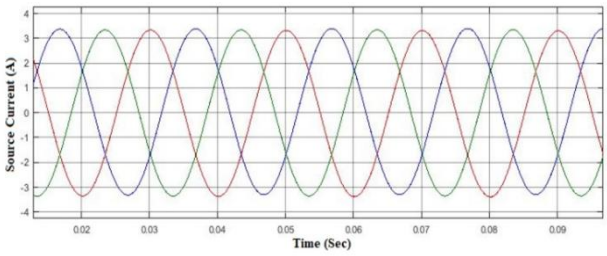


(a) (b)

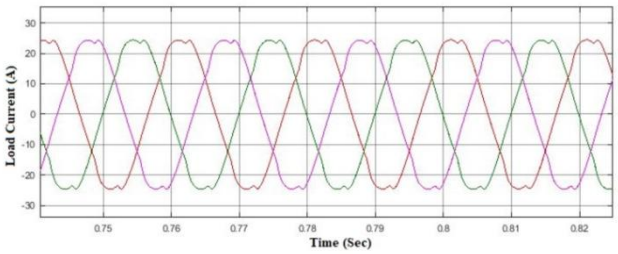
Figure 9. (a) Load current waveform of phase A without a controller. (b) Source current waveform of phase A without a controller.



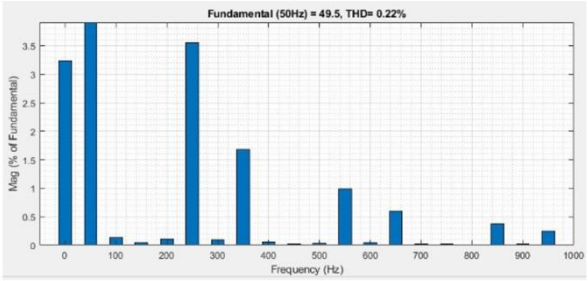
(c)



(d)



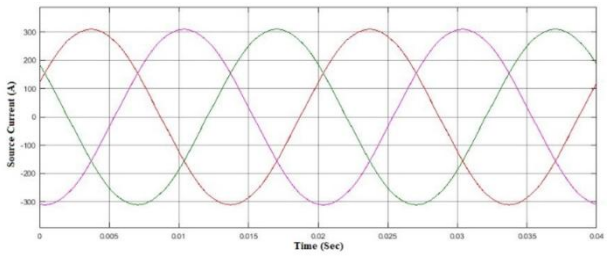
(e)



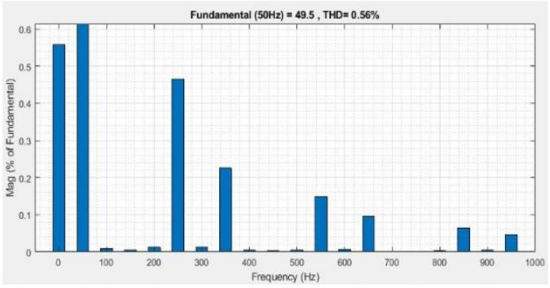
(f)

Figure 9. Continued. (c) Total harmonic distortion (THD) of load current. (d) Source current waveform with passive filter. (e) Load current waveform with passive filter. (f) THD of load current with passive filter.

As seen in Figure 10(a), the hybrid filter is now coupled, and harmonics continue to be reduced when the source current is almost sinusoidal. Improved system efficiency is likewise shown in Figure 10(b) by the use of the hybrid filter, as is the total harmonic distortion.



(a)



(b)

Figure 10. (a) Source current waveform with hybrid filter. (b) System efficiency through usage of the hybrid filter.

As indicated in the Figure 11(a) and Figure 11(b), are the source voltage and source current with DC load connected to the system is shown and also in Figure 11(c) THD is presented in this condition.

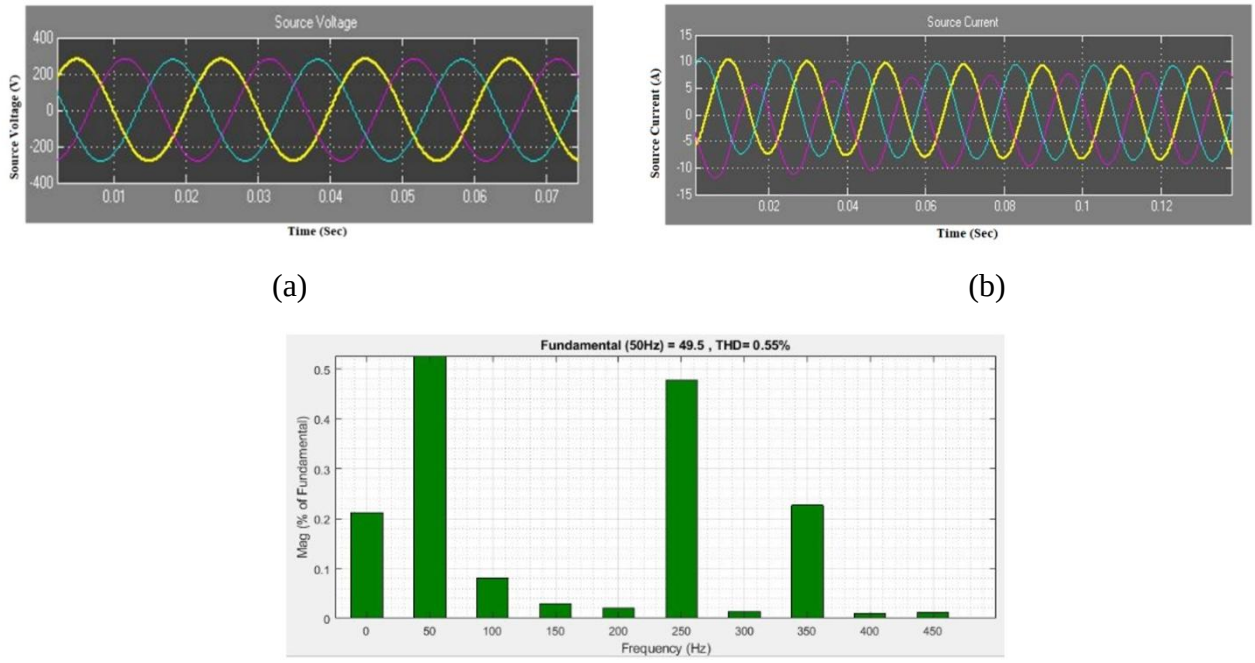


Figure 11. (a) Source voltage waveform with DC load. (b) Source current waveform with DC load. (c) THD associated with connected DC load.

The controller is shown in Figure 1 also, proposed the control strategy of source and load current under unbalanced load conditions. Figure 12(a) and Figure 12(b) demonstrate the simulation result with and without utilizing the hybrid filter [54].

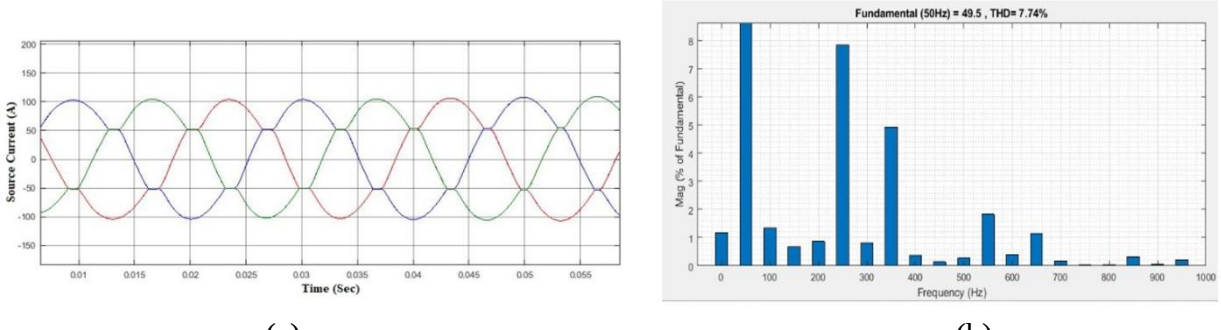
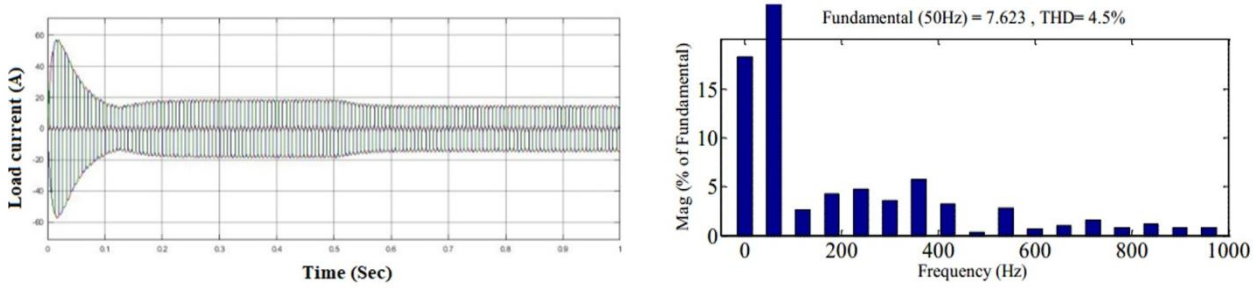


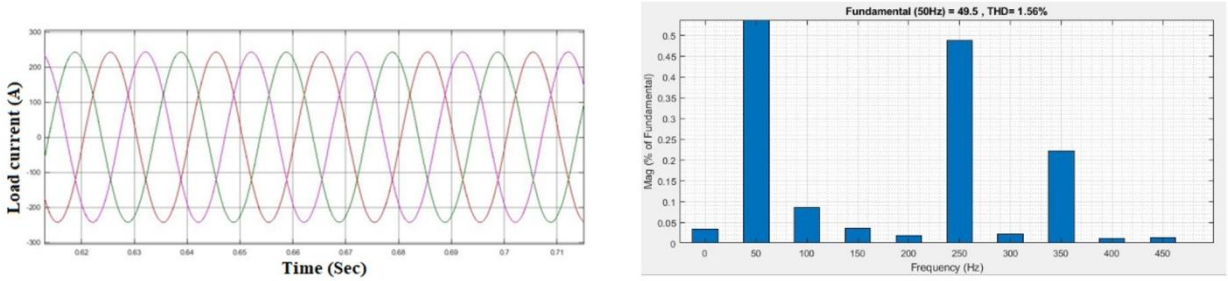
Figure 12. (a) Source current with hybrid filter. (b) THD associated with a hybrid filter.

Thus, the comparison of load current (RL load system) and Total Harmonic Distortion (THD) values with passive and hybrid filters, as well as the comparison of load current for phases A, B, and C with no filter, with a passive filter, as well as the values of THD and power factor for balanced load conditions, as indicated in Table 5, Table 6, and Figure 13 (a), Figure 13 (b), Figure 14 (a), and Figure 14 (b), respectively.



(a) (b)

Figure 13. (a) Load current with no filter. (b) THD associated without a filter.



(a) (b)

Figure 14. (a) Load current with passive filter. (b) THD associated with passive filter.

Table 5. Comparison of load current and THD under balanced load.

Sl. No.	Particulars	THD with passive filter	THD with hybrid filter
1	RL load system	4.8%	1.3%
2	RL load with DC resistor system	3.5%	1.6%

Table 6. Comparison of load current, THD and power factor under balanced load.

Sl. No.	Particulars	THD			Power Factor
		In three phases			
		A	B	C	
1	Load current with no filter	21.45%	33%	35.4%	0.92
2	Load current with passive filter	3.8%	3.3%	4.1%	0.91
3	Load current with hybrid filter	1.21%	1.6%	1.5%	0.96

The above Figure 5 indicates that the L-L-L-G fault happened in the event at the specified fault position B, along with the investigation of RLY_{11} and RLY_{22}'s protection collaboration. Just for the BR_{11}, the RLY_{11} ought to be worked to be open, on the off chance that the fault happens at the B position of the feeder conductor separated with the distributed generator. Nonetheless, fault doesn't happen at the event when BR_{22} is active in its position of feeder conductor linked with the distributed generator. Moreover, the working interval of overcurrent relays is influenced because of

the utilization of the SFCL. In this short circuit analysis of the electric grid including distributed generator coupling, 4 events utilizing the current overcurrent relay, the present directional overcurrent relay, and the overcurrent relay with the projected rectification process were chosen with the thought for the use of the SFCL as follows:

Event 1: utilization of DG including existent overcurrent relays (RLY_{11}, RLY_{22}) in the power distribution network.
Event 2: utilization of DG including existent overcurrent relay (RLY_{11}) and directional overcurrent relay (RLY_{22}) in the power distribution network.
Event 3: utilization of DG including SFCL and existent overcurrent relays (RLY_{11}, RLY_{22}) in the power distribution network.
Event 4: utilization of DG including SFCL and overcurrent relay with recommended rectification process of (RLY_{11}) and existent overcurrent relay (RLY_{22}) in the power distribution network.

In event 4 the implementation of directional overcurrent relay RLY_{22} as supporting the protection of the existent RLY_{22} for application of projected rectification process into the RLY_{11}.

To investigate the activity of overcurrent relays for the above 4 events, a corresponding simulation can be done at 0.35 sec for the occurrence of L-L-L-G fault.

Figure 15 indicates the simulating graphical responses of fault event 1 utilizing the existent overcurrent relays with the distributed generator in the distribution grid. The RLY_{22} functions at 0.543 sec and the RLY_{11} functions at 0.605 sec as depicted with the working feature graphical responses of the overcurrent relay in Figure 6(b). Hence the RLY_{11} ought to function under usual protection. In any event, due to dysfunction of RLY_{22}, causes needless disruption to the feeder conductor dissimilar to the fault. For the action of RLY_{22}, the functioning element of fault current because of distributed generator next to the operation of RLY_{22} appears to diminish, and the slope of coordination value of $RLY_{11}(CRD_{11})$ is marginally altered.

Figure 16 indicates the fault simulation graphical responses of event 2 utilizing the existent overcurrent relay RLY_{11} and the directional overcurrent relay RLY_{22} with DG in the power distribution network. The RLY_{11} functioned at 0.605 sec and the RLY_{22} was not function because of its concealment for the opposite short circuit current. Accordingly, the superfluous disturbing activity because of the dysfunction of the BR_{22} might be obstructed on the event 2.

Figure 17 indicates the fault simulation graphical responses of event 3 utilizing the existent overcurrent relays including the utility of SFCL with DG in the distribution grid. Similar to Figure 5, Figure 17(d) indicates that the performance of fault current restricting activity with the application of SFCL in the top feeder conductor is interrelated with fault incidence. The Figure 15 indicates that for the trip signals (Tr_{11}, Tr_{22}) of overcurrent relays supposedly occurred extra delay at 0.640 sec and 0.620 sec than the incidence time (0.605 sec, 0.543 sec) of the trip signals (Tr_{11}, Tr_{22}), because of the lessening of fault current by current limiter circuit. Nevertheless, tripping signals of the RLY_{22} were yet seen to create initially than the tripping one of the RLY_{11}, as clarified in Figure 6(c) relating to the event 3.

The fault simulation by utilizing the projected amendment strategy for the RLY_{11} was accomplished for repressing the event of reference activity of RLY_{22} earlier the activity of the RLY_{11} despite the lessening of the fault current by the use of the SFCL, as described in Figure 17. Similar to event 4 the simulation responses for the short circuit outcomes including DG and SFCL were displayed in Figure 18 in the power distribution network.

The trip signal of the $RLY_{11}(Tr_{11})$ first happened and the trip signal of the $RLY_{22}(Tr_{22})$

didn't happen with the small variation from the trip signal of the RLY_{22}, as observed in Figure 18(c). However, the integration outcome of (CRD_{22}) keeps on rising till the faulted feeder was isolated, the activity of the RLY_{22} could be discussed to be repressed, therefore the fault feeder line by the point of reference activity of the RLY_{11} was isolated from the fault position.

In event 4 the working interval of the trip signal in $RLY_{11}(Tr_{11})$ was discussed, to be practically similar to the one in event 2 as likened in Figure 16, in which the working repression of the RLY_{22} was implemented as a directional overcurrent relay.

From the investigation on over four events, the safety management of overcurrent relays for the operation of superconducting fault current limiter in a power distribution grid with the distributed generator was affirmed to be advanced over the repression of overcurrent relay dysfunction by implementing the projected rectification technique by the overcurrent relay. Table 7 represents the outcomes of the resulting investigation for four events.

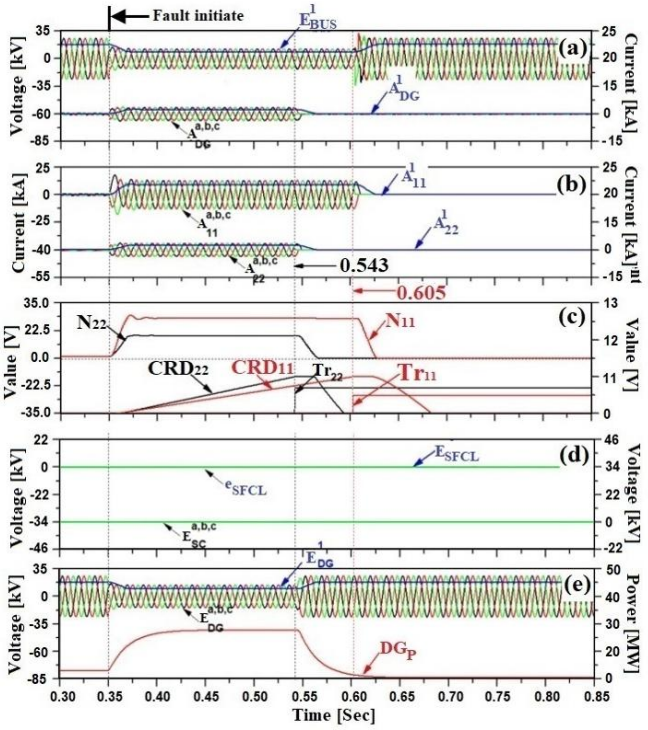


Figure 15. Fault simulation graphical responses for event by utilizing present over current relays $(\mathrm{RLY}_{11}, \mathrm{RLY}_{22})$ in the distribution grid including distributed generator (event 1). (a) Distributed generator current $(\mathrm{A}_{\mathrm{DG}})$ vs bus voltage $(\mathrm{E}_{\mathrm{BUS}})$ responses. (b) line current $(\mathrm{A}_{11}, \mathrm{A}_{22})$ responses (c) activity pointer values $(\mathrm{N}_{11}, \mathrm{N}_{22})$, coordination values $(\mathrm{CRD}_{11}, \mathrm{CRD}_{22})$ and tripping signals $(\mathrm{Tr}_{11}, \mathrm{Tr}_{22})$ of over current relays. (d) High temperature superconductor voltage $(\mathrm{E}_{\mathrm{SC}})$ and SFCL voltage $(\mathrm{E}_{\mathrm{SFCL}})$ (e) Distributed generators active power $(\mathrm{DG}_{\mathrm{P}})$ and voltage $(\mathrm{E}_{\mathrm{DG}})$.

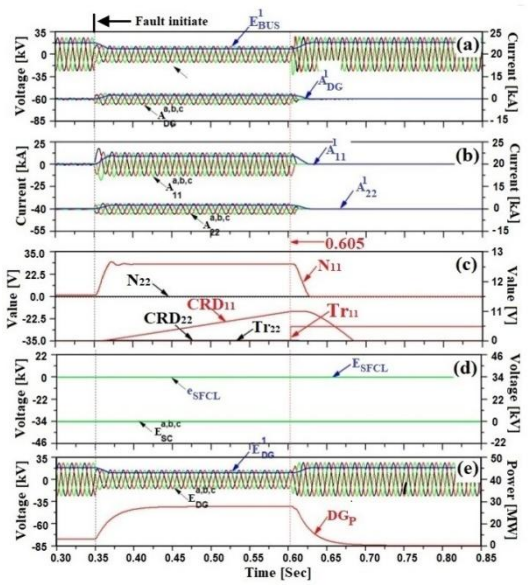


Figure 16. Fault simulation graphical responses for the event by utilizing present overcurrent relay (RLY_{11}) and directional overcurrent relay (RLY_{22}) in the distribution grid including DG (event 2). (a) Distributed generator current (A_{DG}) vs bus voltage (E_{BUS}) responses. (b) line current (A_{11}, A_{22}) responses (c) activity pointer values (N_{11}, N_{22}), coordination values (CRD_{11}, CRD_{22}) and tripping signals (Tr_{11}, Tr_{22}) of overcurrent relays. (d) High-temperature superconductor voltage (E_{SC}) and SFCL voltage (E_{SFCL}) (e) Distributed generators active power (DG_P) and voltage (E_{DG}).

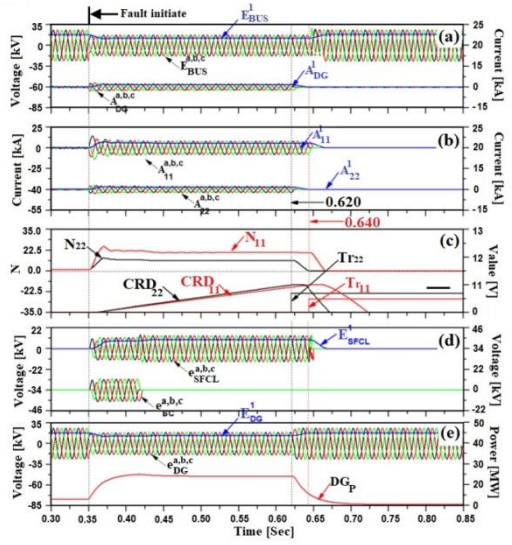


Figure 17. Fault simulation graphical responses for event by utilizing present over current relays (RLY_{11}, RLY_{22}) in the power distribution grid composed of DG and SFCL (event 3). (a) DG current (A_{DG}) vs bus voltage (E_{BUS}) responses. (b) line current (A_{11}, A_{22}) responses (c) activity pointer values (N_{11}, N_{22}), coordination values (CRD_{11}, CRD_{22}) and tripping signals (Tr_{11}, Tr_{22}) of over current relays. (d) High temperature superconductor voltage (E_{SC}) and SFCL voltage (E_{SFCL}) (e) DG active power (DG_P) and DG voltage (E_{DG}).

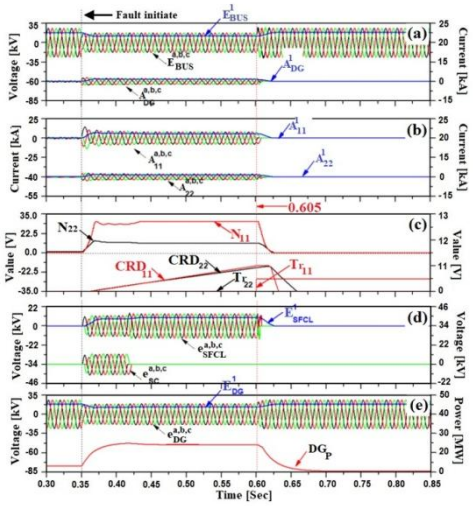


Figure 18. Fault simulation graphical responses for the event by utilizing overcurrent relay with recommended rectification technique (RLY_{11},) and present overcurrent relay (RLY_{22}) in the power distribution grid composed of DG and SFCL (event 4). (a) DG current (A_{DG}) vs bus voltage (E_{BUS}) responses. (b) line current (A_{11}, A_{22}) responses (c) activity pointer values (N_{11}, N_{22}), coordination values (CRD_{11}, CRD_{22}) and tripping signals (Tr_{11}, Tr_{22}) of overcurrent relays. (d) High-temperature superconductor voltage (E_{SC}) and SFCL voltage (E_{SFCL}) (e) DG voltage (E_{DG}) and DG active power (DG_P).

Table 7. Subsequent investigation results of four events.

Event number	Tripping signals of RLY_{11}'s (Tr_{11})(sec)	Tripping signals of RLY_{22}'s (Tr_{22})(sec)	Dysfunction
1	0.605	0.543	Yes
2	0.605	-	No
3	0.640	0.620	Yes
4	0.605	-	No

5. Modelling configuration and flow diagram of proposed distribution grid network

The above Figure 5 used for the simulation and analysis of the working features of overcurrent relay for the proposed power distribution grid network. The distribution grid network comprises of double feeder conductors diverging from the main transformer of 164/32.9 kV. Individual feeder conductor was designed as 20 kilometres, and a loads of 7 [MW] ($Load_{11}$, $Load_{12}$, $Load_{21}$, $Load_{22}$) are connected at each 7 kilometres point. Additionally, circuit breakers (BR_{11}, BR_{12}, BR_{21}, BR_{22}) are placed at a initial point of the feeder conductor and 7 kilometres from the bus conductor. Also, SFCLs ($SFCL_1$, $SFCL_2$) are placed at the initial point of the feeder conductor. Since by dividing the amplitude of the +ve sequence current by the amplitude of the +ve sequence bus voltage, the corresponding system impedance is determined. The total system impedance should be represented by the Eq (24).

Therefore, $N_Z^{'} = \frac{GZ_{Peak}}{\sqrt{\left(R_{feeder} - HR_{SFCL}\right)^2 + \left(X_{feeder} - lR_{SFCL}\right)^2}}$. Where R and X is the system resistance and reactance respectively.

The proposed overcurrent relays functional flow diagram is represented in Figure 19.

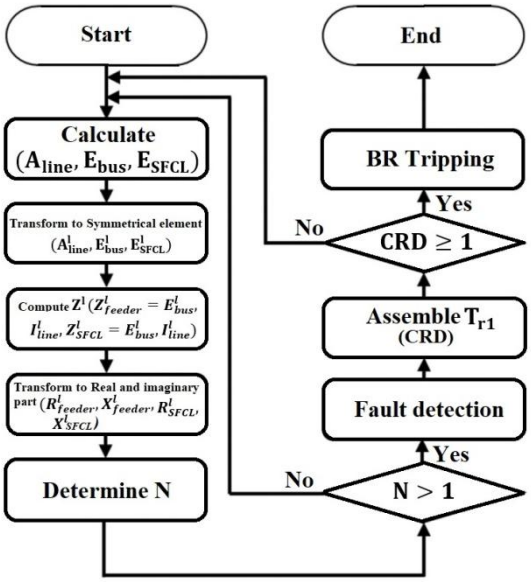


Figure 19. Proposed overcurrent relays functional flow diagram.

Table 8. Comparison of various schemes.

Reference **Key Factor of converters**	**(Xie *et al.*, 2021)**	**(Jiang *et al.*, 2021)**	**(Yehia *et al.*, 2020)**	**(Peddakapu *et al.*, 2018)**	**(Shin *et al.*, 2017)**	**(Jiang *et al.*, 2019)**	**(Li *et al.*, 2020)**	**Proposed Technique**
Switching Topology	Designing of fault-tolerant converters	Reclosing Protection Technique	Stability analysis/Hurwitz criterion	FACTS devices/ distributed power flow controller	voltage sags frequency /reliability analysis technique	MMC-HVdc System	modeling method for dc I-SFCL/ nonlinear characteristic of inductance	Three Phase VSI control (synchronised 6-pulse generator) PWM
Modulation Scheme	PLECS software	PSCAD/EMTDC software	PSCAD/EMTDC software	FACTS controller.	PSCAD/EMTDC software	PSCAD.	Comparison using MATLAB & FEM	Simulink
Power Factor	0.8	Unity	Unity	-	0.9	Unity	-	(0.92, 0.91, 0.96)
THD	N.A	N.A	N.A	N.A	N.A	N.A	N.A	(4.8%, 3.5%)(with passive filter) (1.3%,1.6%)(with hybrid filter)
System Topology	3-phase 4-wire	3-phase 2-wire	5-phase 2-wire	3-phase 2-wire	3-phase 3-wire	3-phase 2-wire	3-phase 4-wire	3-phase 4-wire

A comparison with the several present techniques is shown in the Table 8. However, mainly synchronised 6-pulse generator is used for simulation. The performance in terms of harmonic reduction, power factor, switching technics and hardware/software requirement of the proposed method is demonstrated by Table 8 when compared to other available methods.

6. Sensitivity analysis

It is possible to have a better understanding of the impact of unknown factors on FLC voltage by doing a sensitivity analysis of these parameters in this study. Because the mean value of each parameter has been fixed, sensitivity analysis has been performed on the chosen parameter by altering its value within the range, and the results have been shown in Figure 20 and Figure 21 respectively.

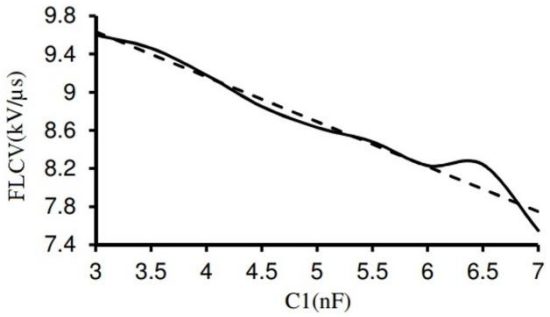


Figure 20. FLCV versus source side capacitance-to-ground (C1).

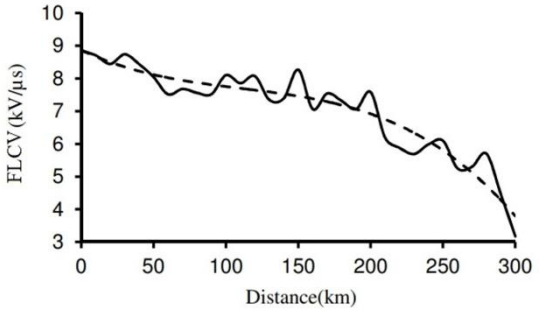


Figure 21. FLCV versus fault distance.

7. Conclusions and future scope

The need for electricity is increasing dramatically, but energy efficiency is the most crucial issue in the energy industry. As a result, it is critical to improve harmonics and the device's strength. The active filter is used in this paper to discuss a way for increasing the efficiency of energy. Along with the active control filter and PCC, the power filter is utilised to connect to the grid. The test is conducted in an unbalanced manner under a variety of operational situations. The hybrid control filter of the APF series improves the strength factor and rising harmonics. The conclusion is that hybrid APF filters and a shunt passive filter are practical and cost-effective methods of improving the electric power system's energy quality.

Additionally, a rectification strategy for the overcurrent relay employing voltage components

was presented in the power distribution network, taking into account the usage of SFCL and the prevention of failure in the overcurrent relay owing to DG linking. To demonstrate the feasibility of the suggested rectification approach, four occurrences involving the use of a fault current limiter in the distribution grid with the distributed generator were selected from the perspective of the existing overcurrent relay and the recommended adjustment strategy. During the investigation of four events of fault analysis from the advanced power distribution grid composed of the distributed generator, it was established that the breakdown of the overcurrent relay in the feeder conductor connected with the distributed generator could be effectively suppressed if the projected revision technique was used.

In future work, the safety management of over-current relays will be developed using the proposed revision strategy, taking into account the DG's utility in the distribution grid's interconnecting area, and the technique for determining the legitimate rectification constants will be recommended in the activity pointer value. The series active power filter coupled VSI regulating approach will be used in greater detail to eliminate harmonics during faults and to enhance the whole power distribution network's power quality. Also, the proposed technique will be investigated by IEEE standard BUS system to prove the feasibility of the proposed system. Additionally, the harmonics elimination technique, power quality improvement, transient stability enhancement, fault current limitation and THD analysis etc. will be investigate by using FACTS devices. Additionally, the renewable and non-conventional energy resources will also be implemented on the proposed technique as a growing platform in the worldwide nation. Afterall in future scope the advanced novel technique will be implemented by the Authors to prove the authenticity and correctness of the proposed technique.

Conflict of interest

The authors declare that there is no conflict of interest.

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