



Research article

Tunnel oxide passivated rear contact for large area *n*-type front junction silicon solar cells providing excellent carrier selectivity

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Abstract: Carrier-selective contact with low minority carrier recombination and efficient majority carrier transport is mandatory to eliminate metal-induced recombination for higher energy conversion efficiency for silicon (Si) solar cells. In the present study, the carrier-selective contact consists of an ultra-thin tunnel oxide and a phosphorus-doped polycrystalline Si (*poly*-Si) thin film formed by plasma enhanced chemical vapor deposition (PECVD) and subsequent thermal crystallization. It is shown that the *poly*-Si film properties (doping level, crystallization and dopant activation anneal temperature) are crucial for achieving excellent contact passivation quality. It is also demonstrated quantitatively that the tunnel oxide plays a critical role in this tunnel oxide passivated contact (TOPCON) scheme to realize desired carrier selectivity. Presence of tunnel oxide increases the implied V_{oc} (iV_{oc}) by ~ 125 mV. The iV_{oc} value as high as 728 mV is achieved on symmetric structure with TOPCON on both sides. Large area (239 cm^2) *n*-type Czochralski (Cz) Si solar cells are fabricated with homogeneous implanted boron emitter and screen-printed contact on the front and TOPCON on the back, achieving 21.2% cell efficiency. Detailed analysis shows that the performance of these cells is mainly limited by boron emitter recombination on the front side.

Keywords: tunnel oxide passivated contact; passivation quality; open-circuit voltage V_{oc} ; back-surface-filed saturation current density J_{ob} ; large area Si solar cell

1. Introduction

As the photovoltaic industry strives towards higher conversion efficiency, technology innovations like carrier-selective passivated contact become important for next generation high-efficiency Si solar cells. This is because these contacts can eliminate high recombination at the metal/Si contact and in the heavily diffused regions [1–4]. Introduction of a thin passivating interlayer between the high recombination regions and the Si absorber mitigates their negative impact because they are not in direct contact with absorber. This reduces total recombination or saturation current density ($J_{0, total}$), resulting in much higher open-circuit voltage V_{oc} . However, the interlayer must passivate the Si surface without interfering with the majority carrier transport to ensure good fill factor (FF) and efficiency. The best example of passivated contact is the heterojunction Si cell with intrinsic thin amorphous layer (HIT). HIT cells have produced outstanding cell V_{oc} of 750 mV [1] with cell efficiency exceeding 25% [2]. However, this passivation scheme can not withstand temperature above 250 °C for the metallization process, and hence is not compatible with the widely used industry standard low-cost screen-printed fired-through metallization, which requires >700 °C temperature for contact-firing. Therefore, our approach to achieve carrier selective contact involves a chemically grown ultra-thin (~ 15 Å) tunnel oxide capped with phosphorus-doped (n^+) polycrystalline Si (*poly*-Si) and metal contact on the entire back side of n -type Si cell, which makes it thermally stable and compatible with low-cost screen-printed metallization.

Figure 1 shows the band diagram of the tunnel oxide passivated contact structure in this study. Three parallel mechanisms contribute to carrier selectivity in this structure. First, heavily doped n^+ *poly*-Si creates an accumulation layer at the absorber surface due to the work function difference between the n^+ *poly*-Si and the n^- Si absorber. This accumulation layer or band bending provides a barrier for holes to get to the tunnel oxide while electrons can migrate easily to the oxide/Si interface. Next, tunnel oxide itself provides the second level of carrier selectivity, because it presents 4.5 eV barrier for holes to tunnel relative to 3.1 eV for electrons [5]. This is the most important carrier selectivity as demonstrated in this study. Third, there are very few or no states on the other side of the dielectric (n^+ region) for holes to tunnel through because of the forbidden gap. Even if some holes are able to tunnel through, they will run into the heavily doped n^+ *poly*-Si layer that offers a barrier for holes to get to the metal contact and recombine. Last but not least, due to the full area metal contact on the back, there is one dimensional current flow. This eliminates the lateral transport resistance in a finished solar cell, resulting in much higher FF .

In this work, we have investigated the influence of the phosphine and silane flow rate ratio (PH_3/SiH_4) during the PECVD deposition of amorphous Si (*a*-Si) film, and the subsequent crystallization and dopant activation anneal temperature on the passivation quality of carrier-selective contact. To study the performance of our passivated contact in a cell, we fabricated large area (239 cm^2) n -type front junction Si solar cells with a boron-doped emitter and screen-printed contact on the front side and the tunnel oxide passivated contact on the rear side (see Figure 2).

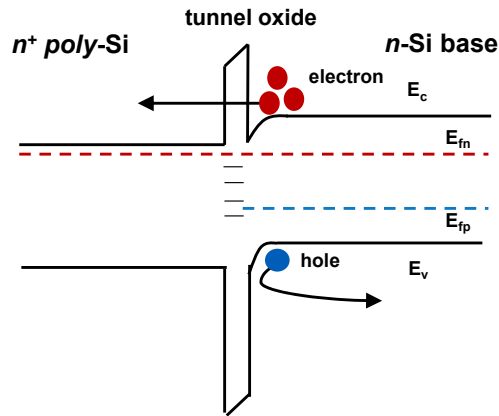


Figure 1. Band diagram of the tunnel oxide passivated contact structure.

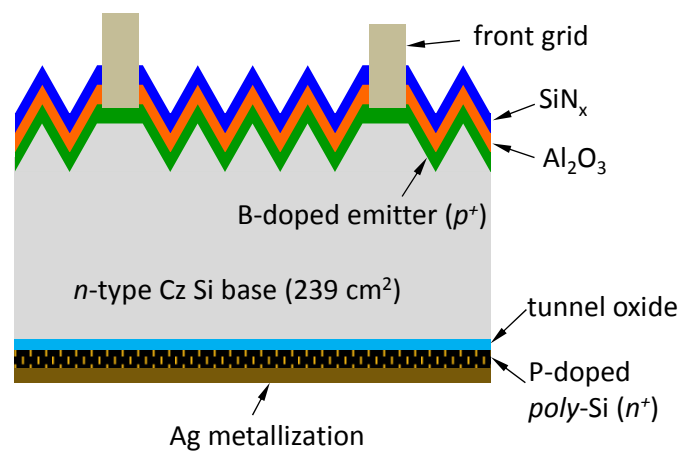


Figure 2. Schematic of the solar cell structure with tunnel oxide/ n^+ poly-Si passivated rear contact and the screen-printed front contact.

2. Materials and Method

The interface quality of passivated rear contact was studied by the quasi-steady state photo-conductance (QSSPC) measurements [6] on symmetrical test structures $\text{Si}(n^+)/\text{SiO}_x/c\text{-Si}(n)/\text{SiO}_x/\text{Si}(n^+)$. Symmetrical samples were made on commercially available n -type Cz wafers with a bulk resistivity of $5 \Omega\text{cm}$ and bulk lifetime of over 2 ms. The sample preparation involved surface damage removal in a heated KOH solution and a RCA chemical cleaning with a resulting wafer thickness of $\sim 170 \mu\text{m}$. The tunnel oxide layer was grown in 68 wt% HNO_3 acid at a temperature of $100 \text{ }^\circ\text{C}$ for 10 min. The resulting tunnel oxide thickness was $\sim 15 \text{ \AA}$, determined by spectral ellipsometry. Next, a thin ($<20 \text{ nm}$) phosphorus-doped Si layer was deposited on both sides using a PECVD tool from Unaxis. Note that both precursors PH_3 and SiH_4 were diluted with H_2 in a volume ratio of 5% for the PECVD a -Si deposition. Then, a $875 \text{ }^\circ\text{C}/30 \text{ min}$ thermal anneal was performed in a tube furnace in an inert atmosphere to facilitate dopant activation and crystallization of a -Si film. The flow rate ratio PH_3/SiH_4 during the PECVD deposition of a -Si film as well as the crystallization temperature was varied in order to study their impact on passivation quality. Finally, the QSSPC

technique [7] was used to determine the passivation quality by extracting the implied V_{oc} (iV_{oc}) from the injection level at one sun according to following equation:

$$iV_{oc} = \frac{kT}{q} \ln \left(\frac{\Delta n(\Delta n + N_D)}{n_i^2} \right), \quad (1)$$

where Δn is the excess carrier density at one sun, k the Boltzmann constant, T the temperature, q the elementary charge, N_D the bulk doping density, and n_i the intrinsic carrier density. The corresponding saturation current density for the back-surface-field region (J_{ob}') was also extracted in the same measurement.

In order to investigate the performance of our rear side tunnel oxide passivated contact in a finished device, large area front junction n -type Si solar cells were fabricated on a $\sim 4.5 \Omega\text{cm}$ Cz wafers (Figure 2). The fabrication process involved saw damage removal in a heated KOH solution followed by alkaline texturing on both sides of the wafers. Next, a SiN_x mask on the front side was deposited, followed by a heated KOH treatment to planarize the back. After the planarization, the wafer thickness was reduced to about $175 \mu\text{m}$. The boron ion implantation with proper dose and energy was performed on a production-line implanter at Suniva Inc. Then, a high temperature anneal ($> 1000 \text{ }^\circ\text{C}$) was used to restore the lattice [8] and eliminate the boron-rich layer formation [9]. The resulting sheet resistivity was $\sim 110 \Omega/\square$ for the boron emitter. Next, the tunnel oxide and n^+ *poly*-Si layers were grown on the rear side according to the process described above. Then a thin Al_2O_3 was deposited by atomic layer deposition (ALD) and capped with PECVD SiN_x film for front surface passivation and anti-reflection coating. The Ag/Al grid was screen-printed on the front, followed by a high temperature firing ($\sim 730 \text{ }^\circ\text{C}$) in an industrial-style belt furnace to achieve good ohmic contact. Finally, $\sim 1 \mu\text{m}$ thick Ag film was deposited by thermal evaporation on the entire rear side.

3. Results and Discussion

In order to obtain an efficiently doped n^+ Si layer to maintain the quasi-Fermi level splitting in c -Si (high V_{oc}), a proper precursor PH_3/SiH_4 flow rate is required to deposit the doped a -Si layer. Figure 3 displays that as the PH_3/SiH_4 flow rate ratio (the doping level of as-deposited a -Si layer) decreases from 8.9% to 4.4%, the iV_{oc} dramatically increases from 678 to 728 mV, and the corresponding J_{ob}' improves from 37.2 to 4.4 fA/cm^2 . This is partly because less phosphorus dopant diffuses from the n^+ Si layer through the tunnel oxide into the c -Si absorber, resulting in reduced Auger recombination. However, as the PH_3/SiH_4 flow rate ratio is further reduced from 4.4% to 1.1% (lower doping in the n^+ *poly*-Si layer), the iV_{oc} declines sharply from 728 to 700 mV, probably due to the reduced doping results in weaker accumulation layer and reduced quasi-Fermi level splitting in the c -Si absorber. The resulting iV_{oc} of 728 mV and J_{ob}' of 4.4 fA/cm^2 at the optimal PH_3/SiH_4 ratio of 4.4% indicate that our tunnel oxide passivated contact structure on Cz Si can provide excellent interface passivation quality for solar cell application, compared to the well-known Yablonovich's semi-insulating polysilicon (SIPOS) solar cell with of J_{ob}' of 10 fA/cm^2 [10] and Feldmann's J_{ob}' value of 8 fA/cm^2 for the TOPCON structure [3] on float-zone (Fz) Si.

After establishing the optimal PH_3/SiH_4 flow rate ratio of 4.4% in our PECVD reactor, we studied the influence of *poly*-Si anneal temperature T_{anneal} ($650 \text{ }^\circ\text{C} \leq T_{anneal} \leq 950 \text{ }^\circ\text{C}$) on the passivation quality. Figure 4 shows a plot of iV_{oc} and J_{ob}' at 1 sun as a function of T_{anneal} . Figure 4 shows that the anneal temperature of $650 \text{ }^\circ\text{C}$ does not change the passivation quality, which remains

quite poor ($iV_{oc} = 645$ mV) and similar to the as-deposited case. As T_{anneal} increases from 650 °C to 875 °C, the passivation quality improves dramatically with iV_{oc} achieving 728 mV. Correspondingly J_{ob}' decreases from 141.5 to 4.4 fA/cm², suggesting that increasing T_{anneal} facilitates the solid-phase crystallization of the as-deposited n^+ α -Si layer [11] and leads to further relaxation or defect healing in the tunnel oxide layer [12]. However, if T_{anneal} increases from 875 °C to 950 °C, a strong degradation in the interface passivation quality is observed, resulting in significant drop in iV_{oc} and increase in J_{ob}' . This is partly due to increase dopant diffusion into Si which increases Auger recombination. This also can lead to local disruption of the tunnel oxide layer, since the gaseous-phase SiO can be produced in N₂ ambient according to the reaction $\text{SiO}_2 + \text{Si} \rightarrow 2 \text{SiO}$. This can result in locally or partially unpassivated Si surface where epitaxial regrowth of the Si layer might happen [13]. Therefore, the role of tunnel oxide layer in our passivated contact structure was studied in the following section.

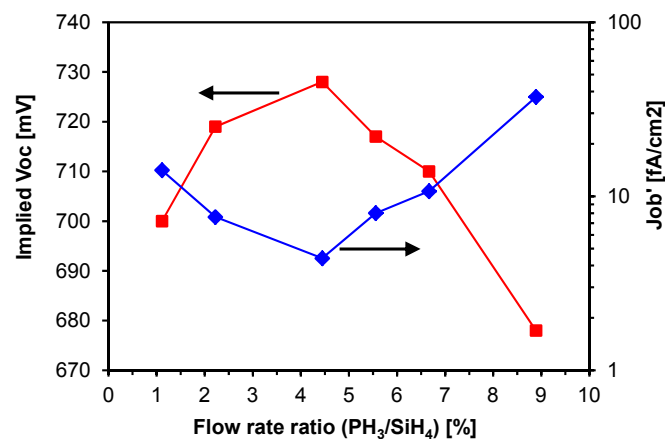


Figure 3. Implied V_{oc} and J_{ob}' as a function of the precursor flow ratio (PH₃/SiH₄). Note that the QSSPC data measured after a 875 °C/30 min anneal. Solid lines are given only as a guide to the eyes.

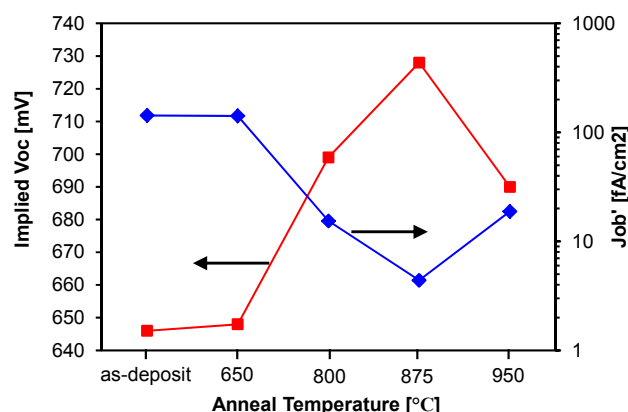


Figure 4. Implied V_{oc} and J_{ob}' as a function of the anneal temperature. Note that the anneal time for each plateau temperature is 30 min. The film right after deposition (“as-deposit”) is also included for comparison purpose. Solid lines are given only as a guide to the eyes.

To investigate the quantitative impact of the tunnel oxide layer on the passivation quality of our structure, two symmetrical test structures were fabricated. One structure has tunnel oxide layer: $\text{Si}(n^+)/\text{SiO}_x/c\text{-Si}(n)/\text{SiO}_x/\text{Si}(n^+)$ and another structure is without tunnel oxide layer: $\text{Si}(n^+)/c\text{-Si}(n)/\text{Si}(n^+)$. This comparison was done with the optimal PH_3/SiH_4 ratio of 4.4% and the optimal T_{anneal} of 875 °C. Figure 5 shows the comparison of injection-dependent effective minority carrier lifetime curves for the two symmetrical test structures (with and without tunnel oxide). The injection level and iV_{oc} at one sun is also shown for the structures. Figure 5 clearly shows that the tunnel oxide layer is crucial for achieving very high quality passivation, since the iV_{oc} drops from 728 to 603 mV and J_{ob}' increases from 4.4 to 1050 fA/cm^2 if tunnel oxide is removed. Hence, the tunnel oxide layer plays as a crucial role in our structure to allow efficient majority carrier (electron in our case) transport while block the minority carrier (hole in our case), because it presents a 4.5 eV barrier for holes to tunnel relative to 3.1 eV for electrons. In this study a symmetrical test structure capped with just the tunnel oxide ($\text{SiO}_x/c\text{-Si}(n)/\text{SiO}_x$) was also fabricated to evaluate the passivation quality of tunnel oxide by itself. The test structure gave a very low iV_{oc} of 653 mV and a high J_{ob}' of 92 fA/cm^2 , indicating that the back surface field (BSF) induced by fixed charge in the tunnel oxide layer does not provide sufficient surface passivation.

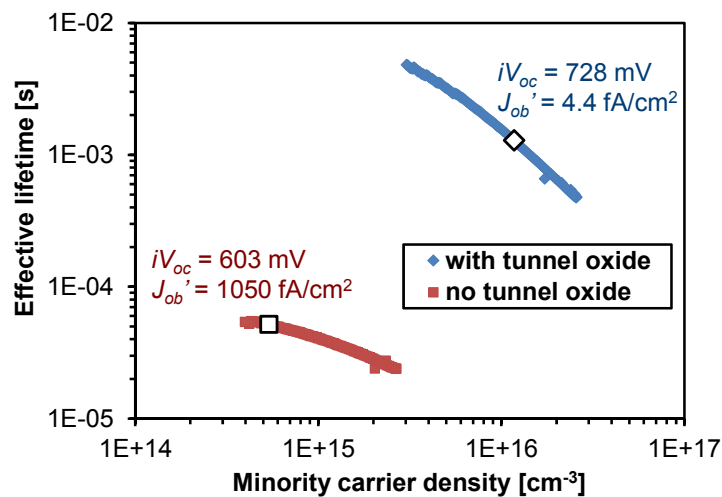


Figure 5. Comparison of injection dependent effective minority carrier lifetime for the symmetrically passivated samples with and without the tunnel oxide layer. The figure also depicts the injection level at one sun and the corresponding iV_{oc} and J_{ob}' .

In order to quantify the impact of tunnel oxide on cell performance, solar cells were fabricated with ion-implanted homogeneous boron emitter on the front and passivated contact on the back with and without tunnel oxide (Figure 2). Table I lists the corresponding solar cell results, which was measured at AM 1.5G, 100 mW/cm^2 , 25 °C, using the Fraunhofer ISE certified 20.2% efficient large area n -type cell [14] as a reference. The highest V_{oc} of 683 mV was achieved with the tunnel oxide passivated structure, supporting excellent rear passivation quality. The cells also showed a high average short-circuit current density J_{sc} of 39.5 mA/cm^2 and average cell efficiency of 21.0%, with the highest of 21.2%. However, the cells without tunnel oxide layer showed very low V_{oc} of ~ 625 mV, and efficiency of less than 19%. This is mainly due to the extremely high J_{ob}' of

$\sim 1050 \text{ fA/cm}^2$ that limits its V_{oc} to $\leq 625 \text{ mV}$, as also indicated by the simple one-diode model equation for Si solar cells:

$$V_{oc} = \frac{nkT}{q} \ln \left(\frac{J_{sc}}{J_{0e} + J_{0b}} + 1 \right), \quad (2)$$

where $J_{0e} = J_{0e, pass} + J_{0e, metal}$, and $J_{0b} = J_{0b, bulk} + J_{0b}'$. Note that $J_{0e, pass}$ is emitter saturation current density of $\text{Al}_2\text{O}_3/\text{SiN}_x$ passivated boron emitter, which was measured as $\sim 24 \text{ fA/cm}^2$ using the QSSPC measurement on the unmetallized symmetrical emitter structure ($\text{SiN}_x/\text{Al}_2\text{O}_3/p^+/n/p^+/\text{Al}_2\text{O}_3/\text{SiN}_x$) [15]. $J_{0e, metal}$ is the metal grid contribution to saturation current density, which was modeled at $\sim 50 \text{ fA/cm}^2$ based on the Sentaurus simulation program [16,17]. $J_{0b, bulk}$ is $\sim 25 \text{ fA/cm}^2$ for 2 ms bulk lifetime base. Hence, the dominant recombination for the cells with tunnel oxide passivated contact is attributed to the front side, since J_{0e} ($= J_{0e, pass} + J_{0e, metal} = 24 + 50 = 74 \text{ fA/cm}^2$) $\gg J_{0b}'$ ($= 4.4 \text{ fA/cm}^2$). Therefore, it can be concluded that the V_{oc} of the cells with tunnel oxide passivated contact can be improved further by introducing a selective emitter underneath the metal contact. In addition, the significantly lower internal quantum efficiency (*IQE*) in the long wavelength range of 900–1200 nm (see Figure 6) due to the high back surface recombination velocity for the cells without tunnel oxide layer also supports the resulting much lower V_{oc} and inferior J_{sc} , compared to the cells with tunnel oxide layer. Furthermore, very comparable internal reflection in the long wavelength range for both structures in Figure 6 indicates that there is negligible free carrier absorption in the tunnel oxide layer [18], which is desired for an excellent light trapping at rear side.

Table 1. Comparison of the I - V parameters of large area n -type front junction Si solar cells featuring passivated rear contact with and without tunnel oxide layer.

Passivated contact structure	Cells	V_{oc} [mV]	J_{sc} [mA/cm ²]	FF [%]	Efficiency [%]
with tunnel oxide	Average (4 cells)	678.1 ± 5.3	39.5 ± 0.2	78.9 ± 0.8	21.0 ± 0.2
	Best	683.4	39.7	78.1	21.2
without tunnel oxide	Average (3 cells)	623.4 ± 1.9	38.4 ± 0.2	78.3 ± 0.5	18.6 ± 0.2
	Best	625.3	38.5	78.4	18.8

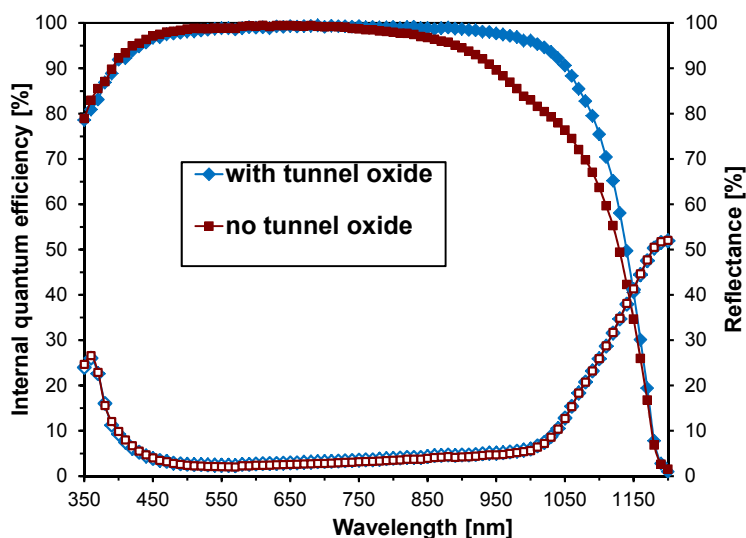


Figure 6. Comparison of internal quantum efficiency (*IQE*) and reflectance of the cell featuring rear contact structure with and without tunnel oxide layer.

4. Conclusion

High-efficiency tunnel oxide passivated large area *n*-type front junction Si solar cells are presented. It has been shown that the passivation quality of our passivated contact scheme depends strongly on the precursor PH_3/SiH_4 flow rate ratio (hence the doping level of n^+ Si layer) and the subsequent crystallization and dopant activation anneal temperature. Optimization of process parameters enabled an iV_{oc} of as high as 728 mV with the corresponding J_{ob}' value of 4.4 fA/cm^2 , suggesting an excellent interface passivation quality. Furthermore, an extremely high J_{ob}' value of over 1000 fA/cm^2 for the structure solely passivated by the n^+ *poly*-Si layer reveals that the tunnel oxide layer plays a critical role to provide carrier selectivity in our studied structure. The finished cells with tunnel oxide passivated rear contact showed average cell efficiency of over 21% after screen-printed metallization on a homogeneous ion-implanted boron emitter, demonstrating the promise of this technology option for industrial production of high-efficiency Si solar cells.

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Conflict of Interest

All authors declare no conflict of interest in this paper.

References

1. Taguchi M, Yano A, Tohoda S, et al. (2013) 24.7% record efficiency HIT solar cell on thin silicon wafer. *Proceedings of the 39th IEEE Photovoltaic Specialist Conference*, Tampa, Florida, USA, pp. 96–99.
2. Masuko K, Shigematsu M, Hashiguchi T, et al. (2014) Achievement of more than 25% conversion efficiency with crystalline silicon heterojunction solar cell. *IEEE J Photovoltaics* 4: 1433–1435.
3. Feldmann F, Bivour M, Reichel C, et al. (2014) Passivated rear contacts for high-efficiency n-type Si solar cells providing high interface passivation quality and excellent transport characteristics. *Sol Energy Mater Sol Cells* 120: 270–274.
4. Heng JB, Fu J, Kong B, et al. (2015) >23% high-efficiency tunnel oxide junction bifacial solar cell with electroplated Cu gridlines. *IEEE J Photovoltaics* 5: 82–86.
5. Lee WC, Hu CM (2001) Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence-band electron and hole tunneling. *IEEE Trans Electron Devices* 48: 1366–1373.
6. Sinton RA, Cuevas A, Stuckings M (1996) Quasi-steady-state photoconductance, a new method for solar cell material and device characterization. *Proceedings of the 25th IEEE Photovoltaic Specialists Conference*, Washington D.C., USA, pp. 457.
7. Kane DE, Swanson RM (1985) Measurement of the emitter saturation current by a contactless photoconductivity decay method (silicon solar cells). *Proceedings of the 18th IEEE Photovoltaic Specialists Conference*, Las Vegas, Nevada, USA, pp. 578–583.
8. Hermle M, Benick J, Rüdiger M, et al. (2011) N-type silicon solar cells with implanted emitter. *Proceedings of the 26th European Photovoltaic Solar Energy Conference*, Hamburg, Germany, pp. 875.
9. Tao Y, Rohatgi A (2014) High-efficiency large area ion-implanted n-type front junction Si Solar cells with screen-printed contacts and SiO₂ passivated boron emitters. *Proceedings of the 40th IEEE Photovoltaic Specialists Conference*, Denver, Colorado, USA, pp. 3654–3658.
10. Yablonovitch E, Gmitter T, Swanson RM, et al. (1985) A 720 mV open circuit voltage SiO_x:c-Si:SiO_x double heterostructure solar cell. *Appl Phys Lett* 47: 1211–1213.
11. Feldmann F, Simon M, Bivour M, et al. (2014) Efficient carrier-selective p- and n-contacts for Si solar cells. *Sol Energy Mater Sol Cells* 131: 100–104.
12. Nemeth B, Young DL, Yuan H, et al. (2014) Low temperature Si/SiO_x/pc-Si passivated contacts to n-type Si solar cells. *Proceedings of the 40th IEEE Photovoltaic Specialist Conference*, Denver, Colorado, USA, pp. 3488–3452.
13. Wolstenholme GR, Jorgensen N, Ashburn P, et al. (1987) An investigation of the thermal stability of the interfacial oxide in polycrystalline silicon emitter bipolar transistors by comparing device results with high-resolution electron microscopy observations. *J Appl Phys* 61: 225–233.
14. Tao Y, Ok Y-W, Zimbardi F, et al. (2014) Fully ion-implanted and screen-printed 20.2% efficient front junction silicon cells on 239 cm² N-type Cz substrate. *IEEE J Photovoltaics* 4: 58–63.
15. Hoex B, Schmidt J, Bock R, et al. (2007) Excellent passivation of highly doped p-type Si surfaces by the negative-charge-dielectric Al₂O₃. *Appl Phys Lett* 91: 112107.

16. Renshaw J, Kang MH, Meemongkolkiat V, et al. (2009) 3D-modeling of a back point contact solar cell structure with a selective emitter. *Proceedings of the 34th IEEE Photovoltaic Specialists Conference*, Philadelphia, Pennsylvania, USA, pp. 375–379.
17. Altermatt PP (2011) Models for numerical device simulations of crystalline silicon solar cells—a review. *J Comput Electron* 10: 314–330.
18. Bivour M, Reichel C, Hermle M, et al. (2012) Improving the a-Si:H(p) rear emitter contact of n-type silicon solar cells. *Sol Energy Mater Sol Cells* 106: 11–16.



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